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MS-7719

Version: 0A **Lenovo**

CPU: Intel Tunnel_Creek

System Chipset:

Intel Top Cilff

On Board Device:

Clock Gen - ICS/ICS9LPRS436 & 9DB403

Super I/O - SMSC SCH5147

CPLD - Altera EPM570

LAN - REALTEK/RTL8111E

HD Audio Codec -- REALTEK/ALC887

SVDO to DVI Interface

SVDO to VGA Interface(Reserve)

LVDS Scalar

Main Memory:

DDR2 1GB 667MHz

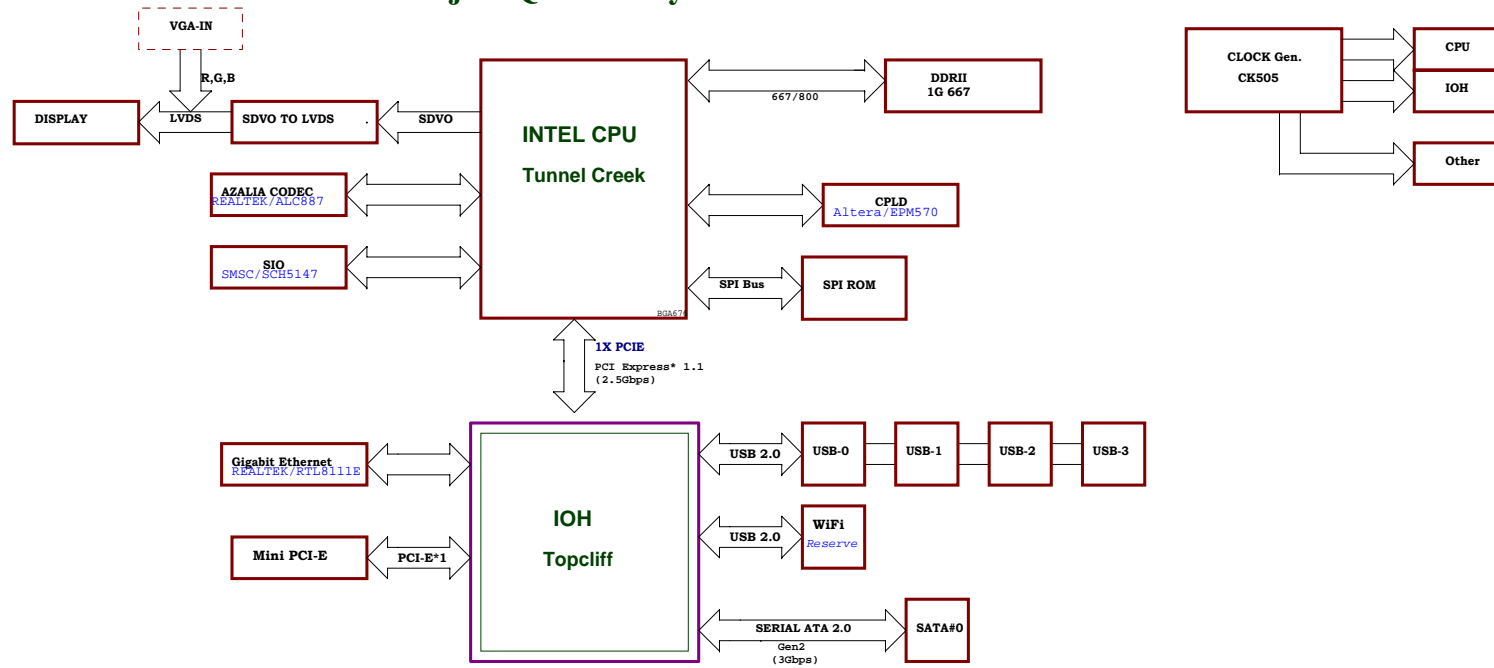
PWM: ON Semi/ADP3211

SLOT: Mini PCIE SLOT



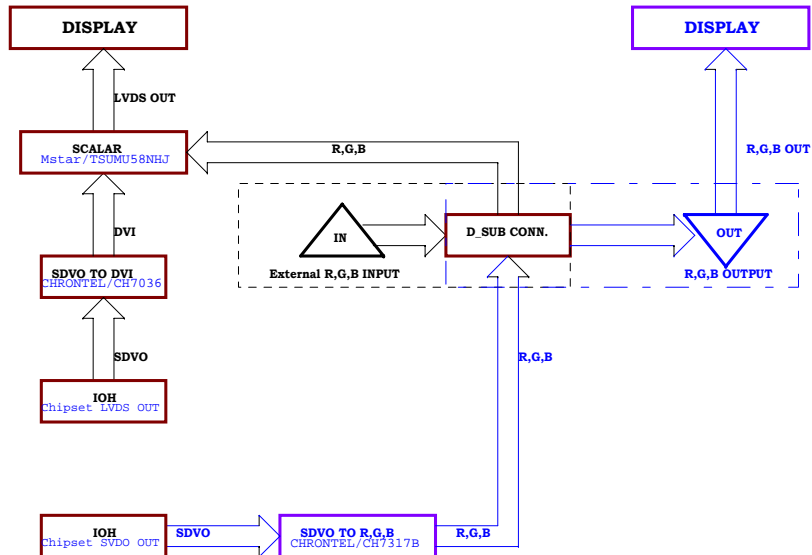
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MS-7719		
Size Custom	Document Description Cover Sheet	Rev 0A
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Project Queens Bay BLOCK DIAGRAM



DISPALY BLOCK DIAGRAM

21.5"



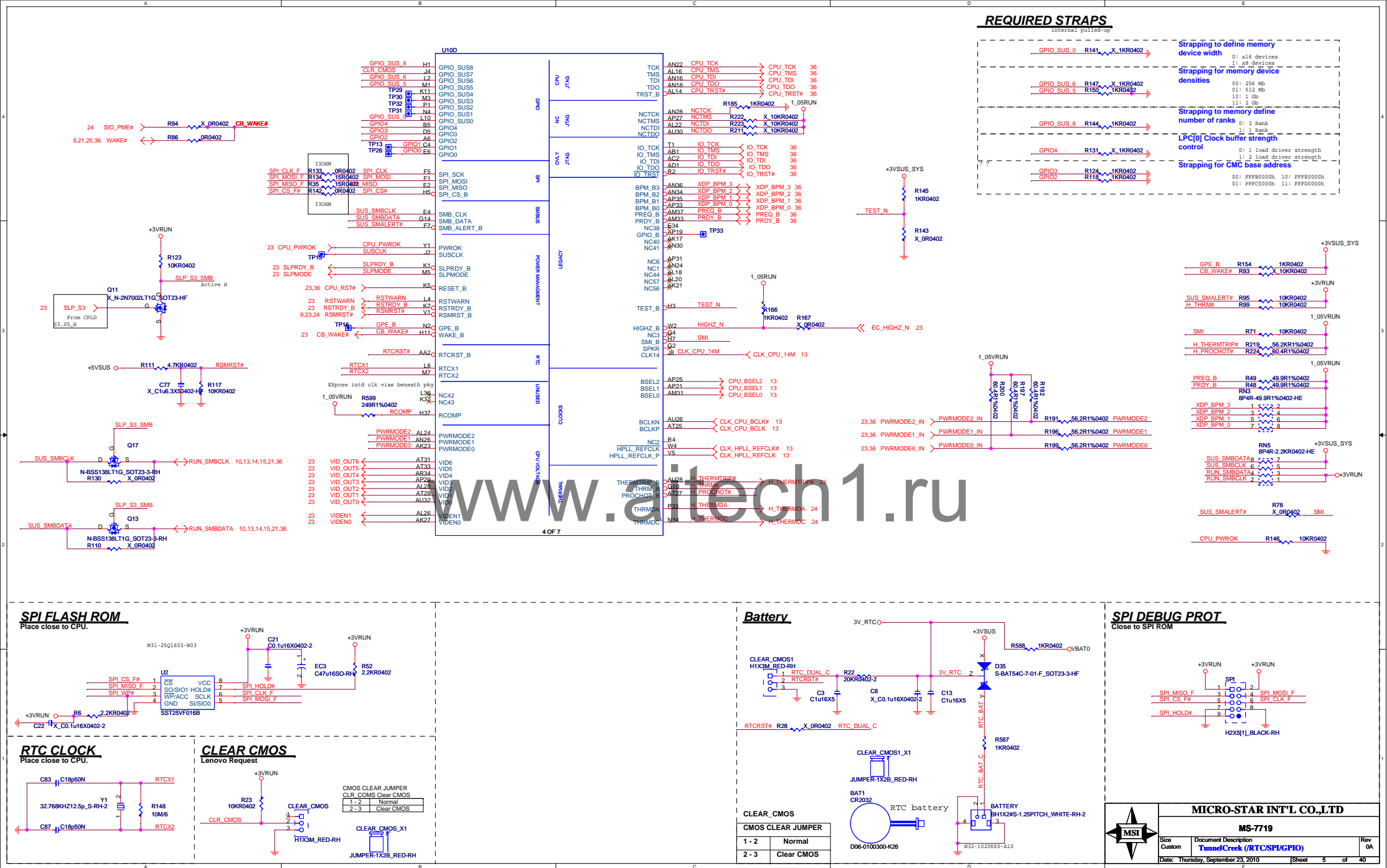
40"

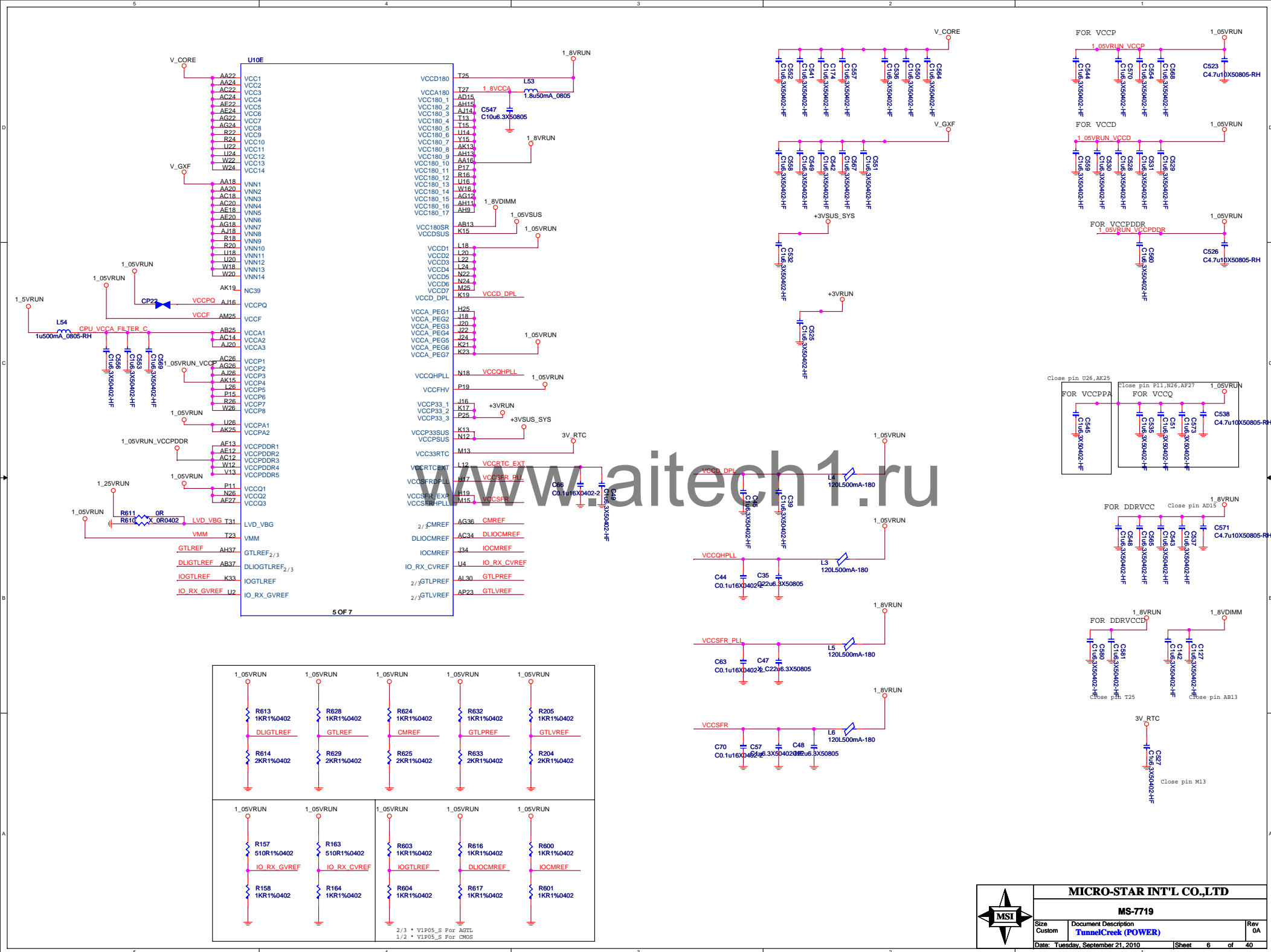


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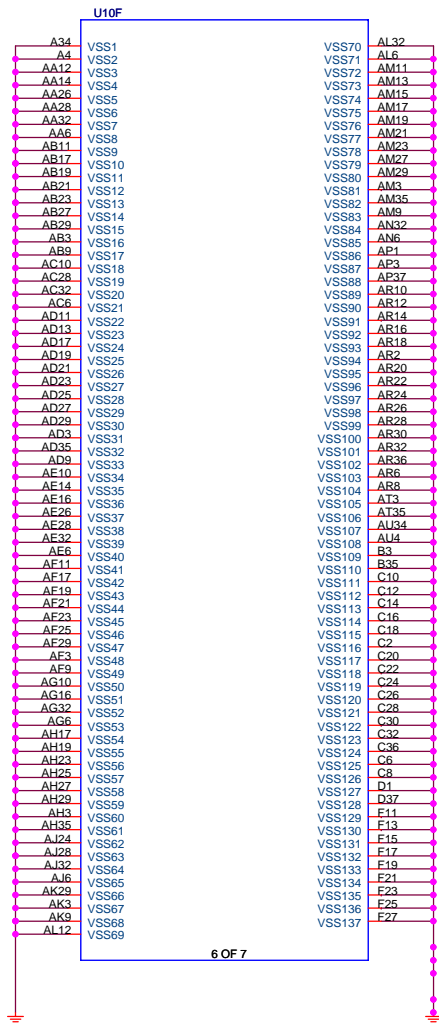
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Size	Custom
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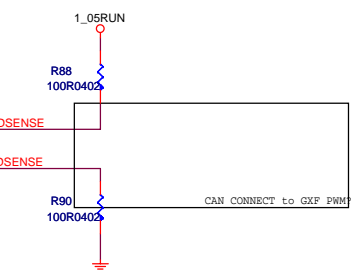
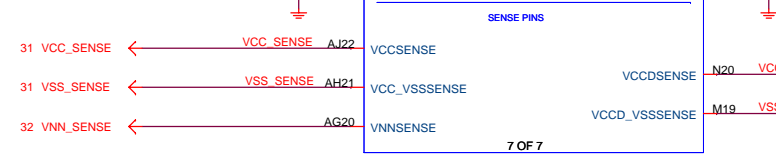
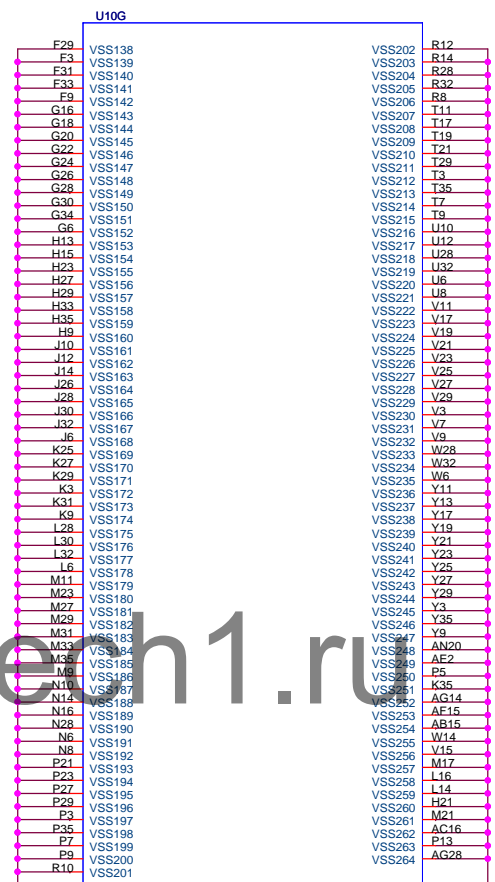
Size Custom	Document Description TunnelCreek (POWER
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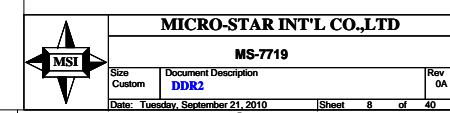


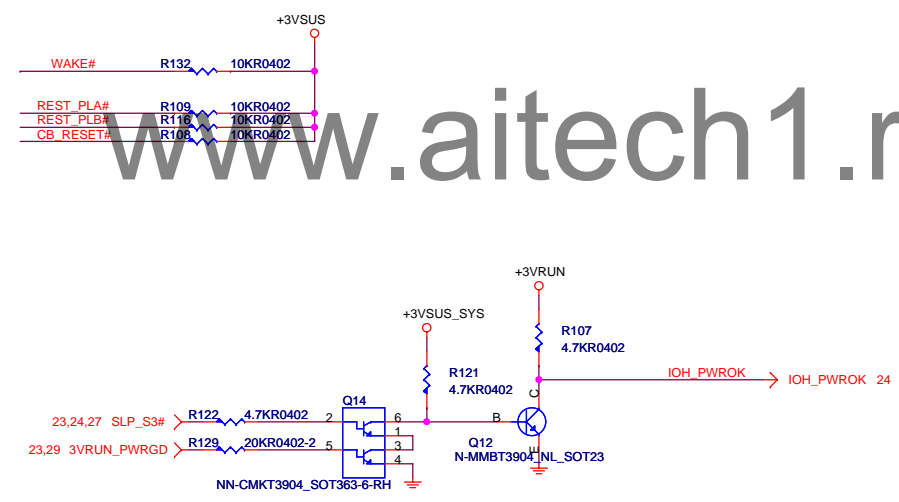
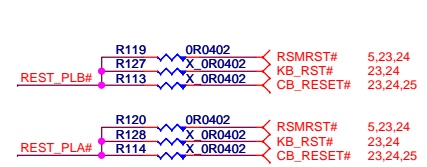
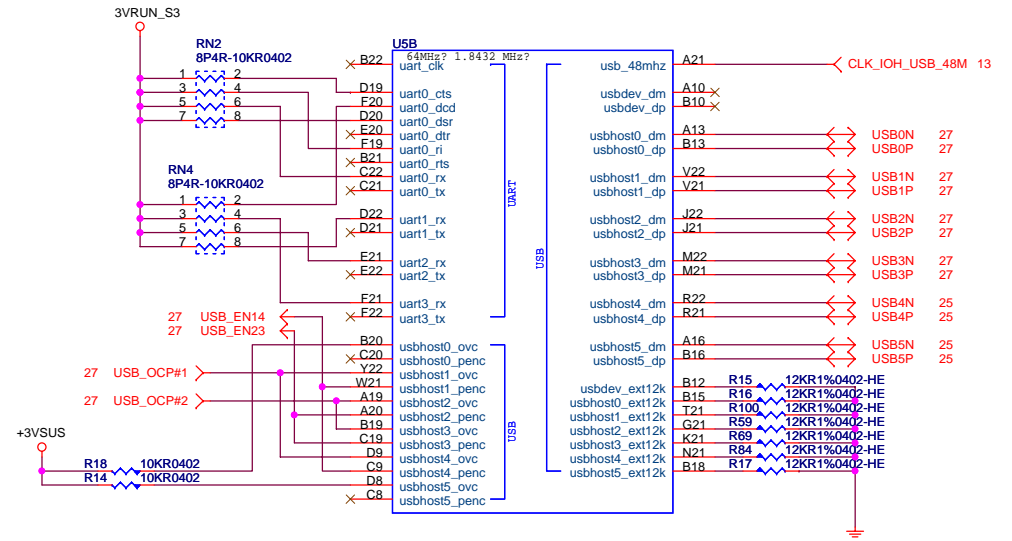
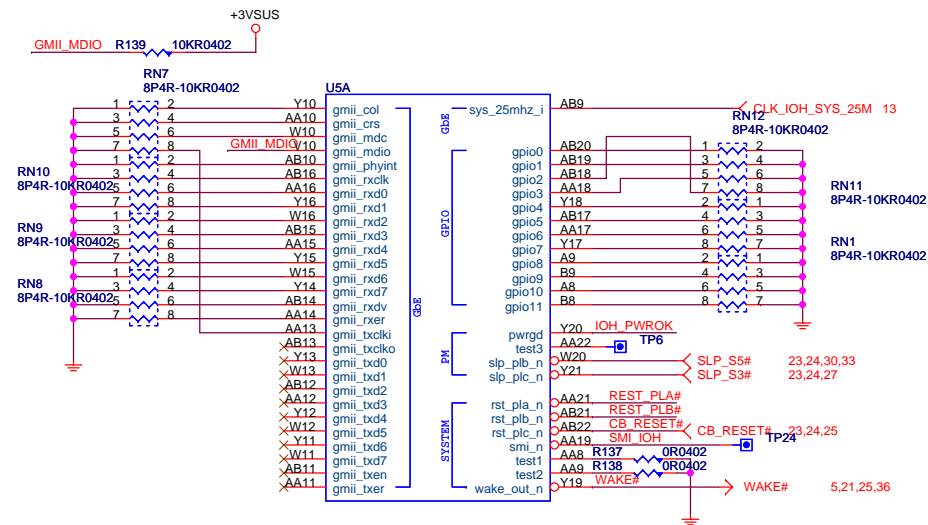
1G/667

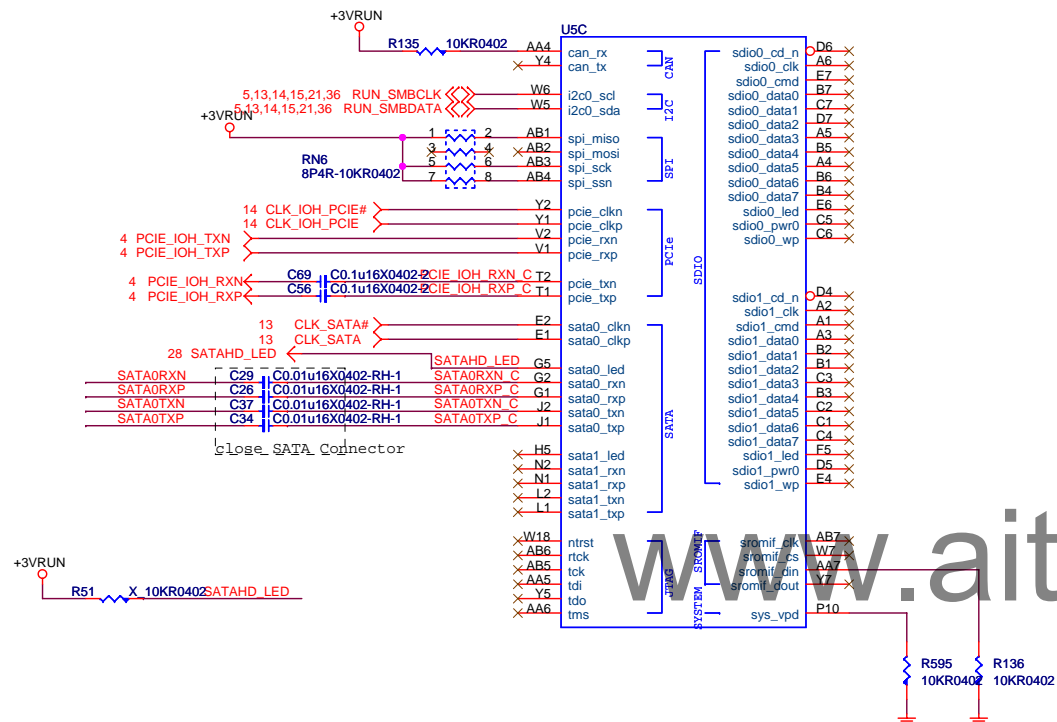
1G/667



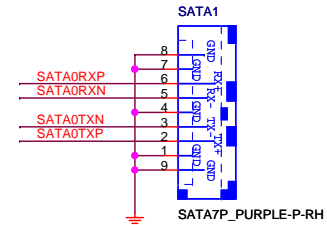
DDR2 TREMINATION



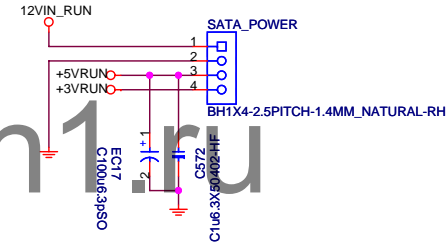




SATA HDD CONN



spinup (Max) 1A

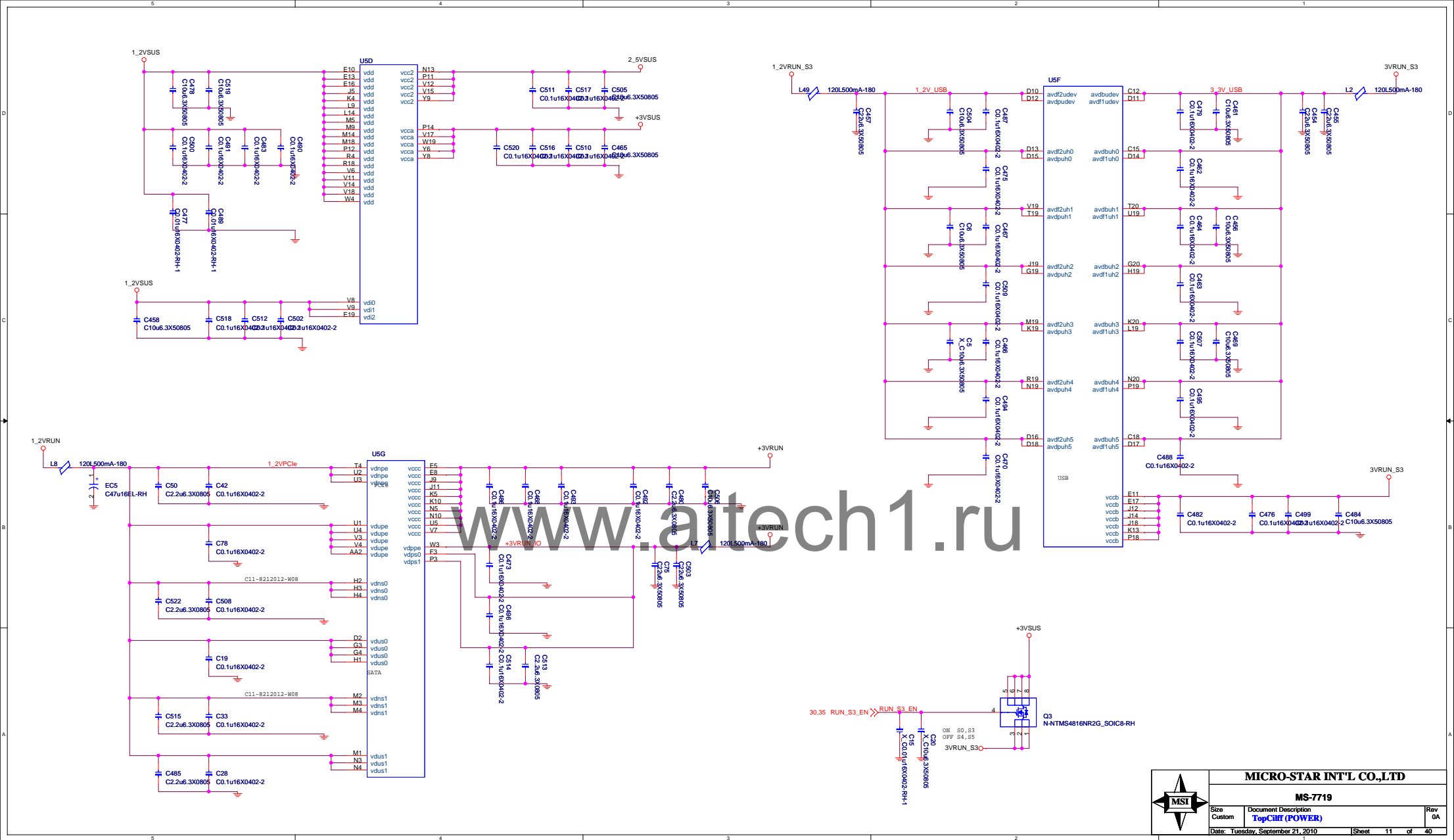


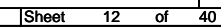
MICRO-STAR INT'L CO.,LTD

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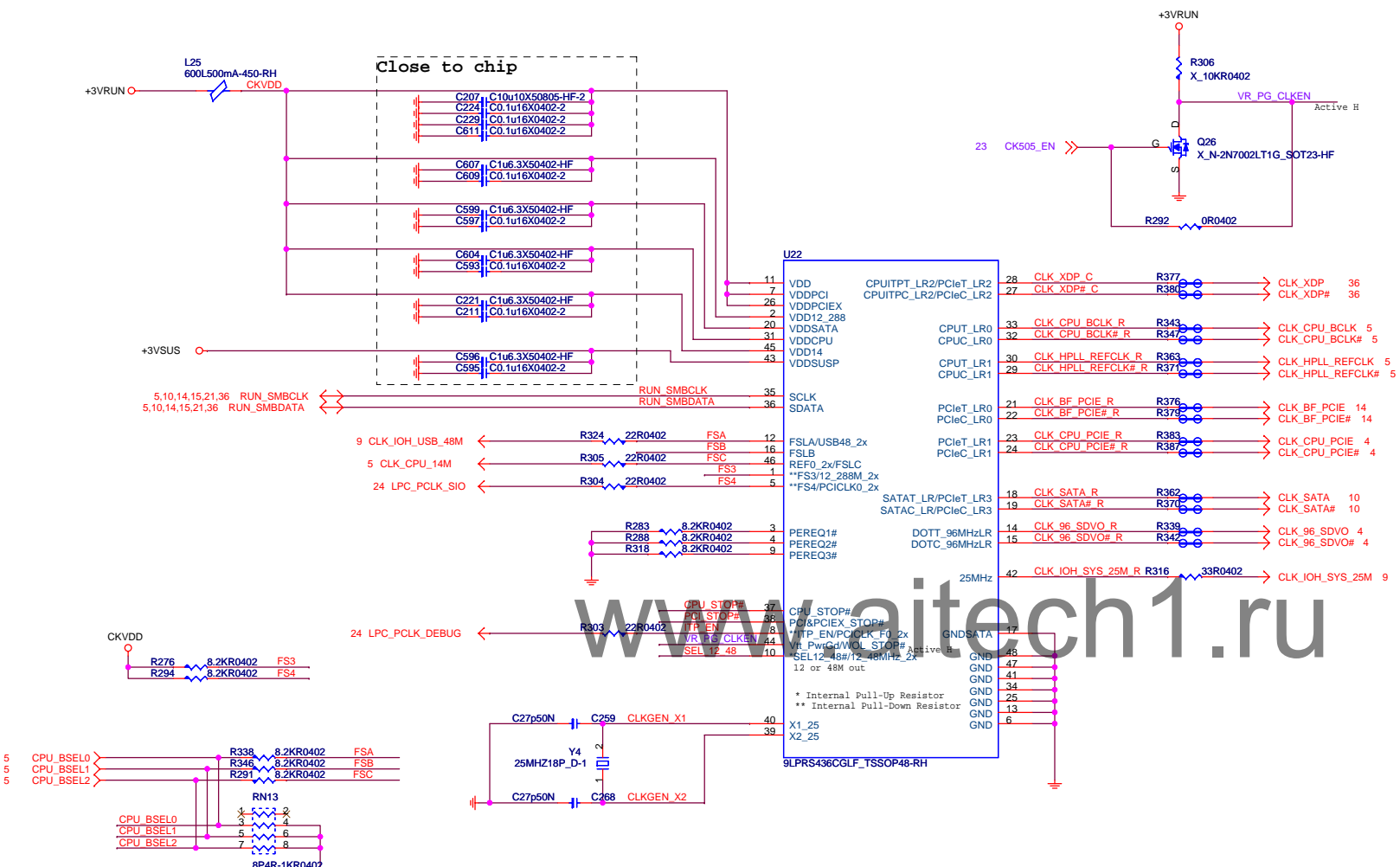
Size	Document Description	Rev
Custom	TopGilt (SATA/SDCard)	0A

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CLK Gen ICS9LPRS436



CPU Table			
FSC	FSB	FSA	BCLK
(Only L for Tunnel Creek A0)	H	L	83.33MHZ
(Only H for Tunnel Creek A0)	H	L	83.33MHZ
H	L	L	100MHZ
L	L	L	100 MHz

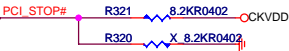
CLK Gen			
BSEL[0]	BSEL[1]	BSEL[2]	BCLK
L	H	L	83.33MHZ
H	H	L	83.33MHZ
L	L	L	100 MHz
H	L	L	100 MHz

CLOCK GEN STRAPING

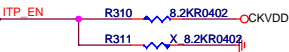
Stops CPU0 clock when enabled.



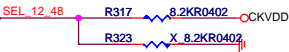
Stops all PCICLKs at logic 0 level, when low. Free running PCICLKs are not effected by this input.




ITP Enable Latched Input/Free Running PCI clock output. ITP_Enable Selects the functionality of the CPU_ITP/SRC output as follows:
1 = CPU_ITP output
0 = SRC output



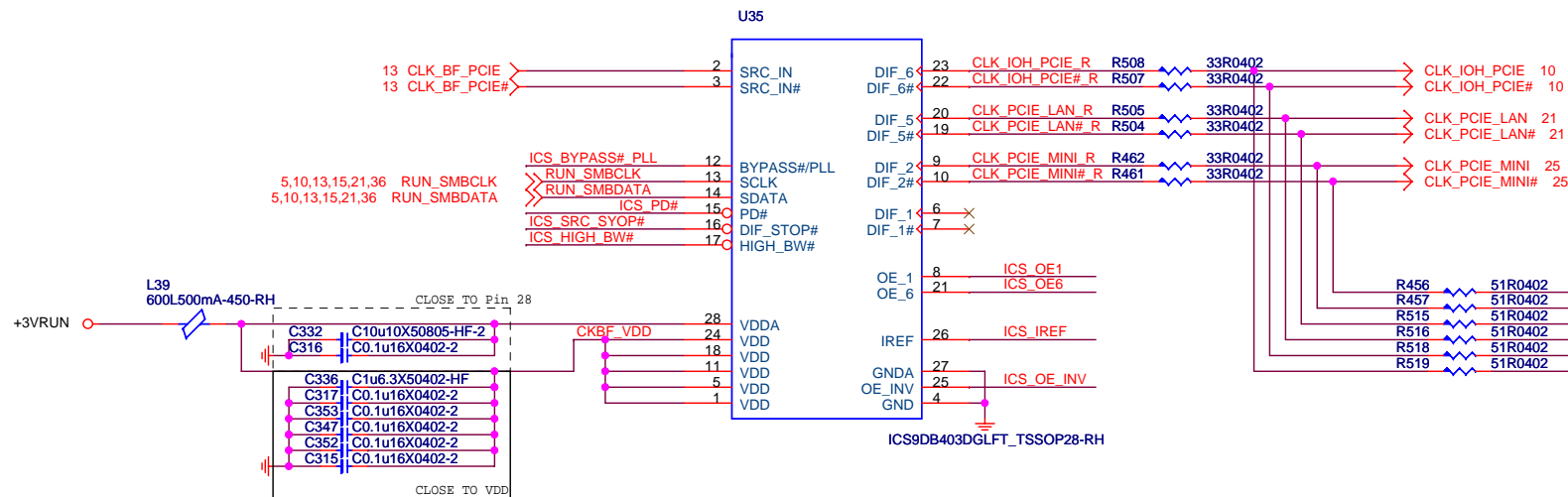
Latched select input for 12/48MHz output.
1=12MHz
0=48MHz
12/48MHz Output





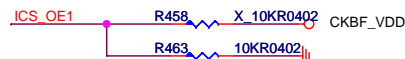
MICRO-STAR INT'L CO.,LTD		
MS-7719		
Size Custom	Document Description CLK GEN - ICS9LPRS436	Rev 0A
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CLK Buffer ICS9DB403DG



STRAPPING

Active high input for enabling output 1.
0 = tri-state outputs, 1= enable outputs



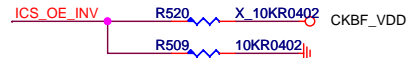
Input to select Bypass (fan-out) or PLL (ZDB) mode
0 = Bypass mode, 1= PLL mode



Active high input for enabling output 6.
0 = tri-state outputs, 1= enable outputs



This latched input selects the polarity of the OE pins.
0 = OE pins active high, 1 = OE pins active low (OE#)



3.3V input for selecting PLL Band Width
0 = High, 1= Low



Active low input to stop differential output clocks.



This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.

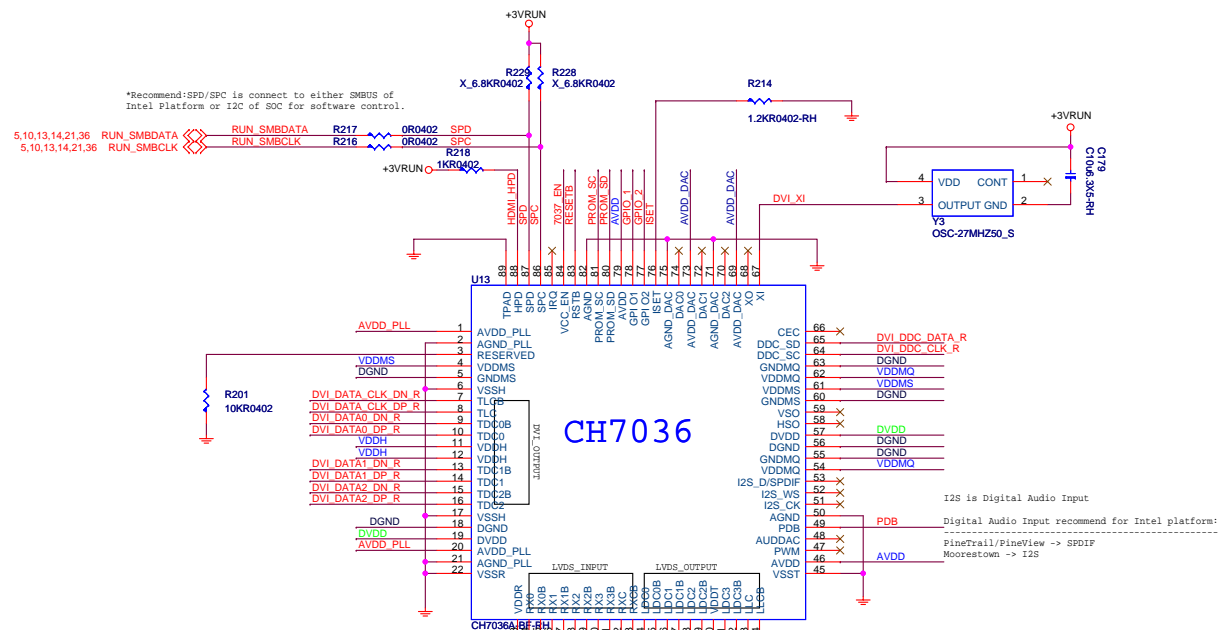


Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal osc. (if any) are stopped.

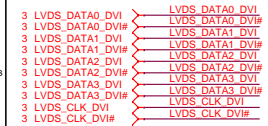


MICRO-STAR INT'L CO.,LTD			
MS-7719			
Size Custom	Document Description CLK BUFFER - ICS9DB403		Rev 0A
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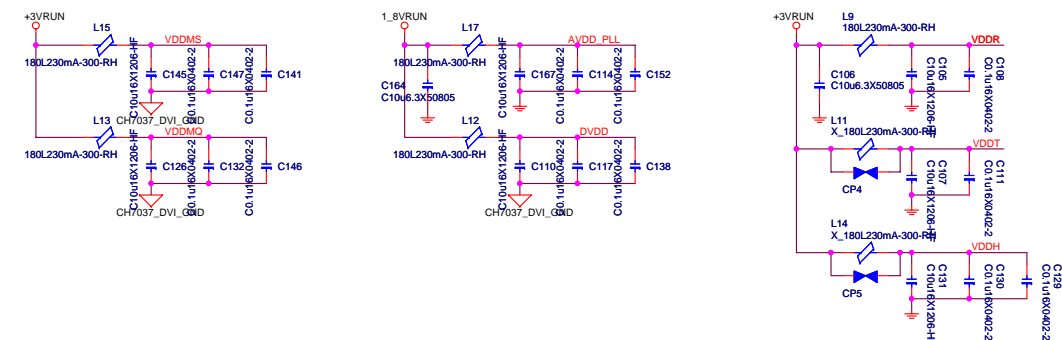
LVDS To DVI ENCODER



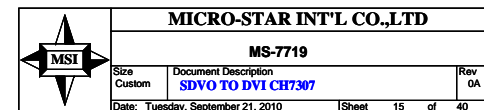
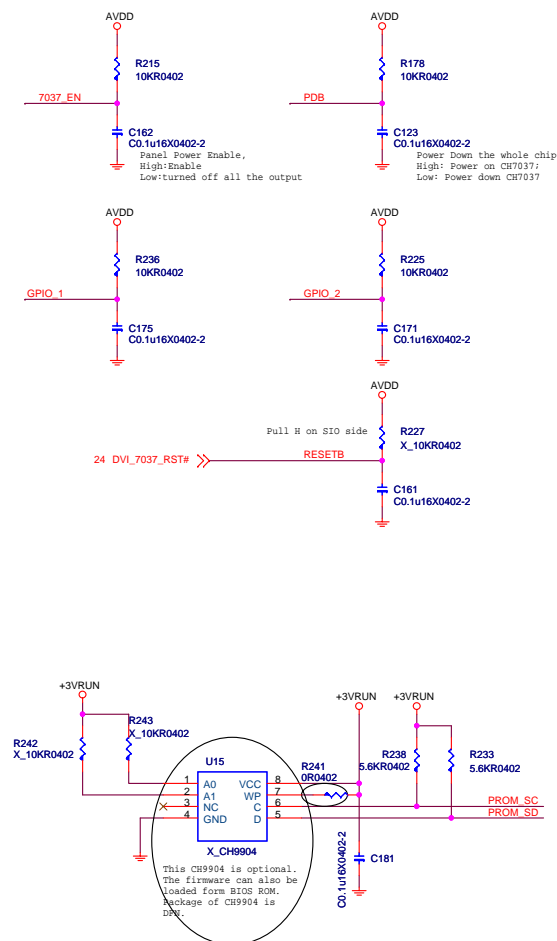
<i>LVDS Input</i>



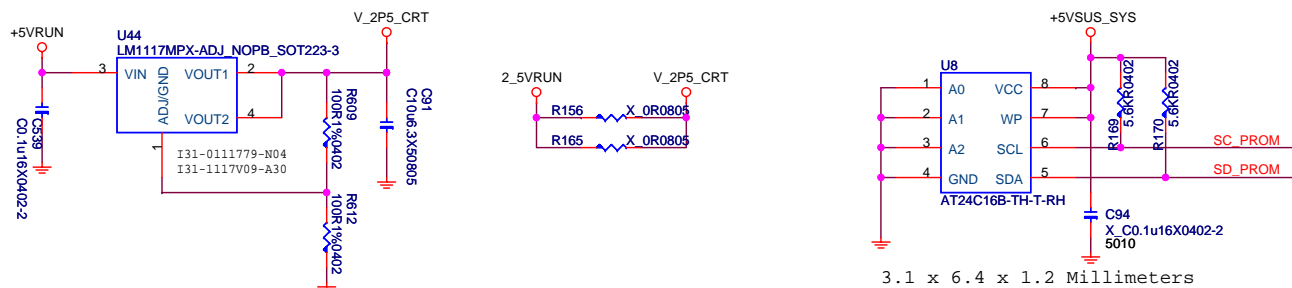
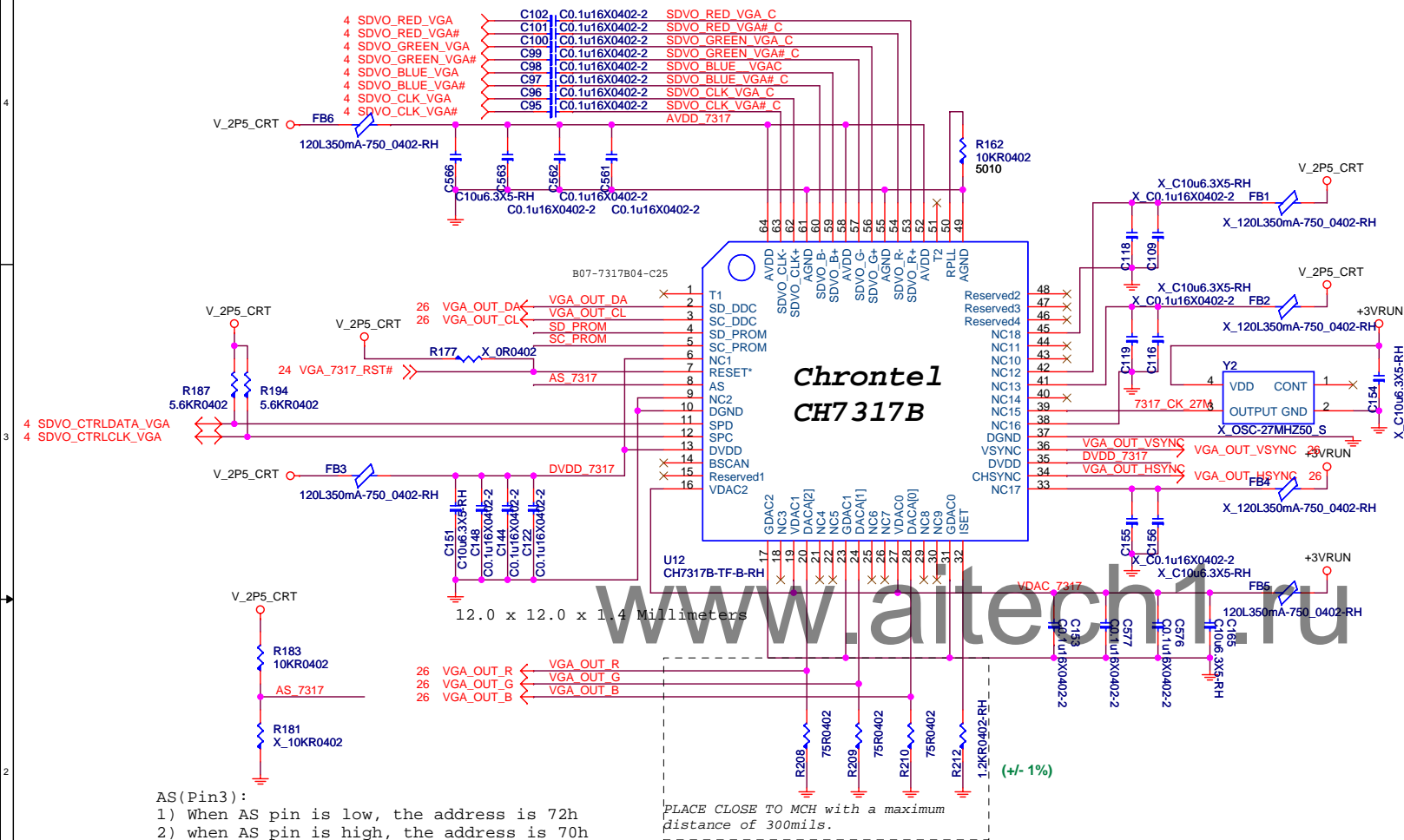
POWER



STRAPS



SDVO To VGA CONTROLLER

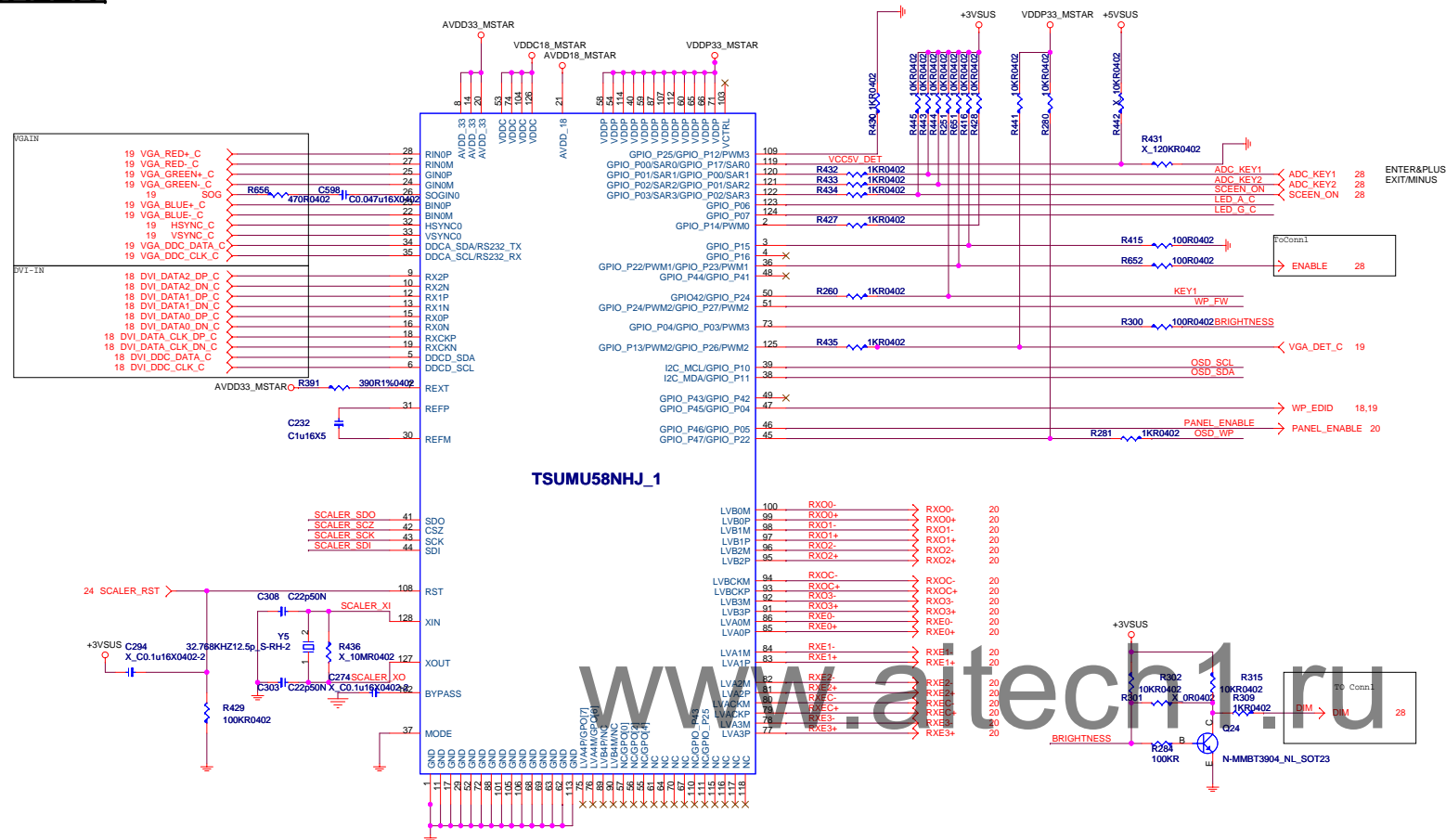


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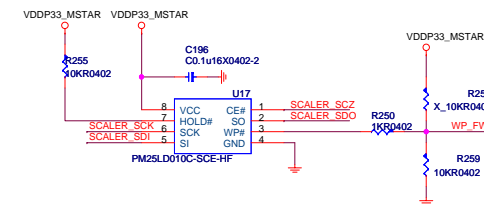
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Size Custom	Document Description SDVO TO VGA CH7317B	Rev 0A
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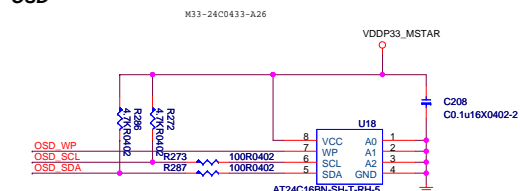
SCALER



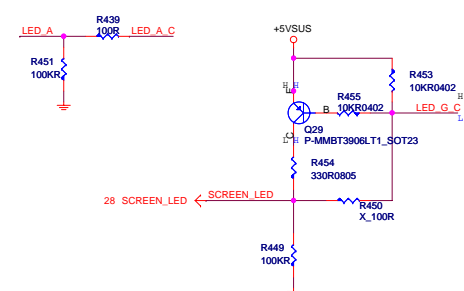
SPI



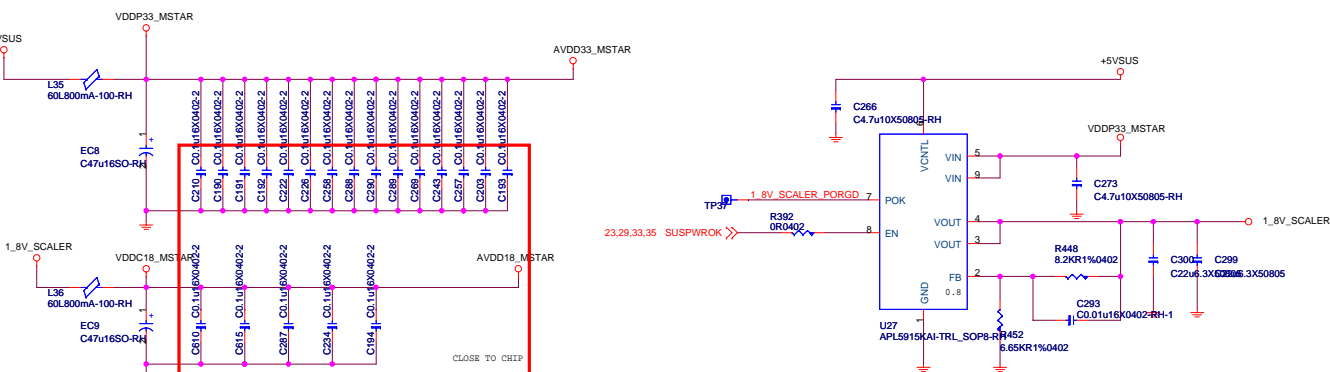
OSD



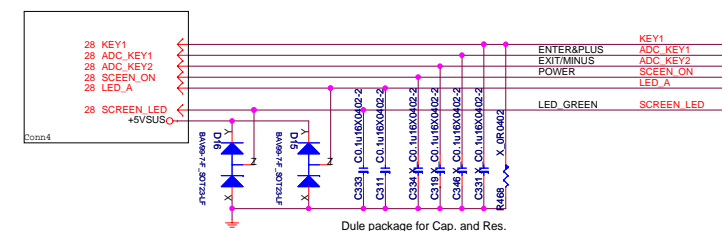
LED



POWER



To Keypad



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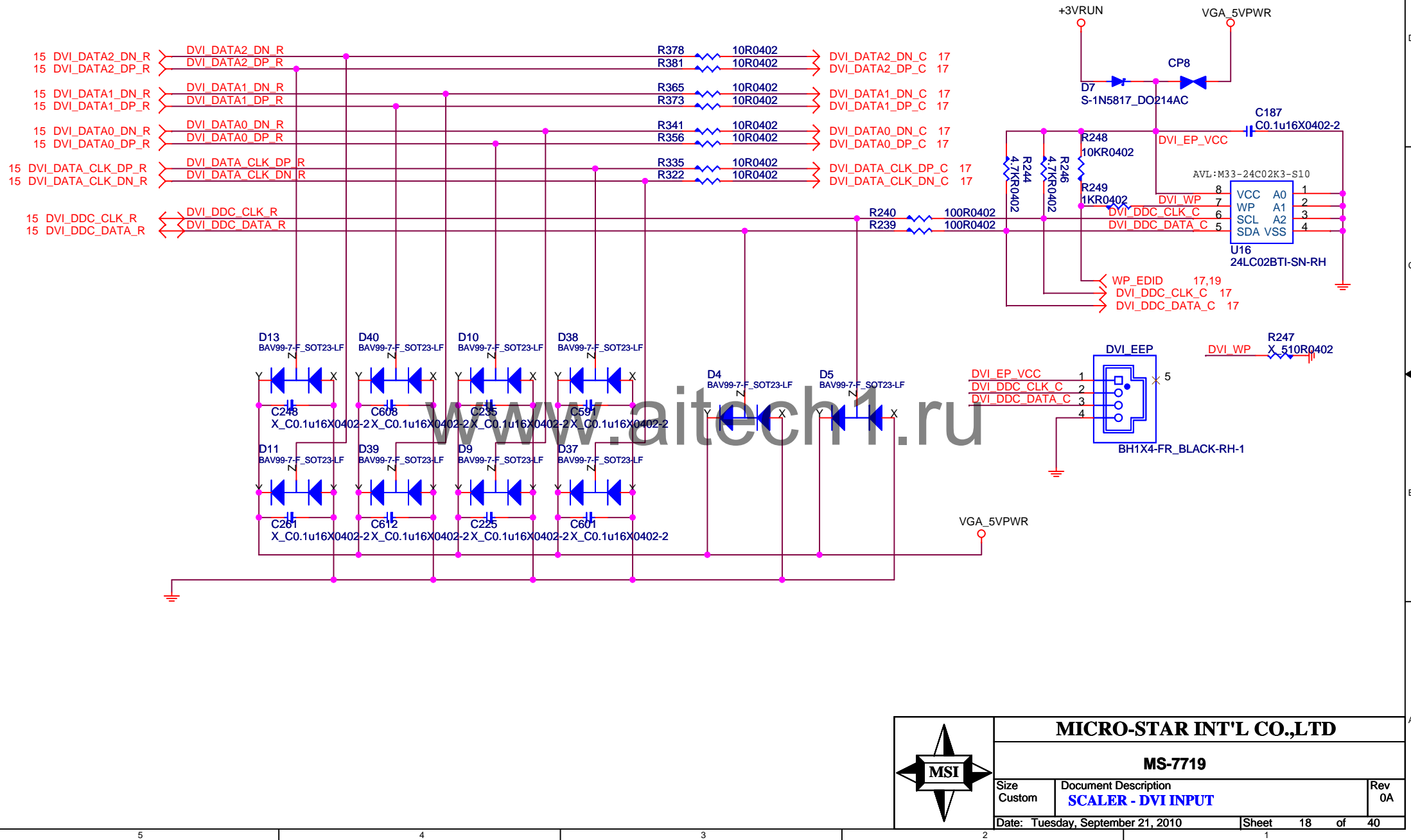
MS-7719	
Size	Document Description

Size	Document Description	Rev
Custom	SCALER - MSTAR/TSUMU58NHJ	0A

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DVI INPUT

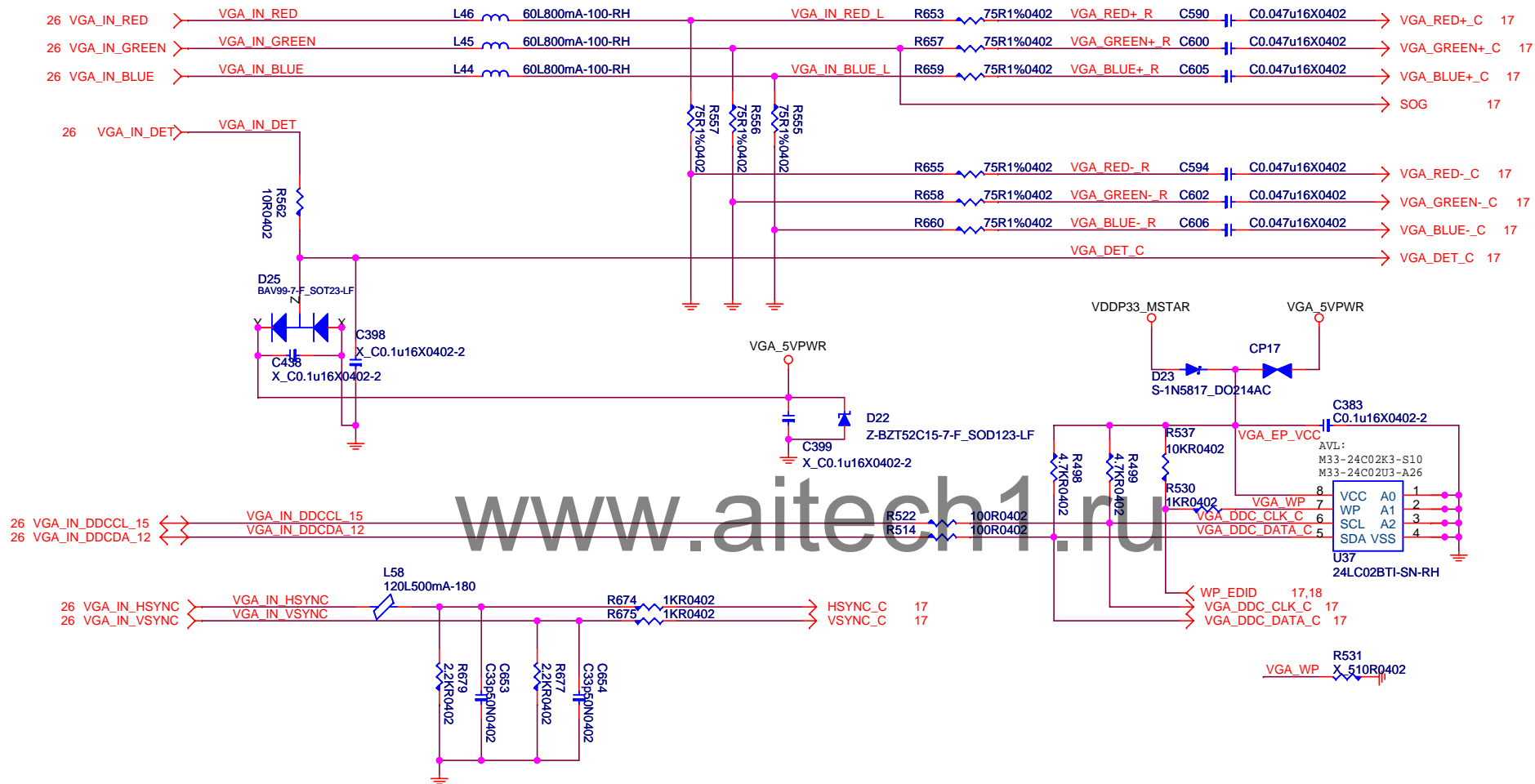
From CH7307




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	Size Custom	Document Description SCALER - DVI INPUT	Rev 0A
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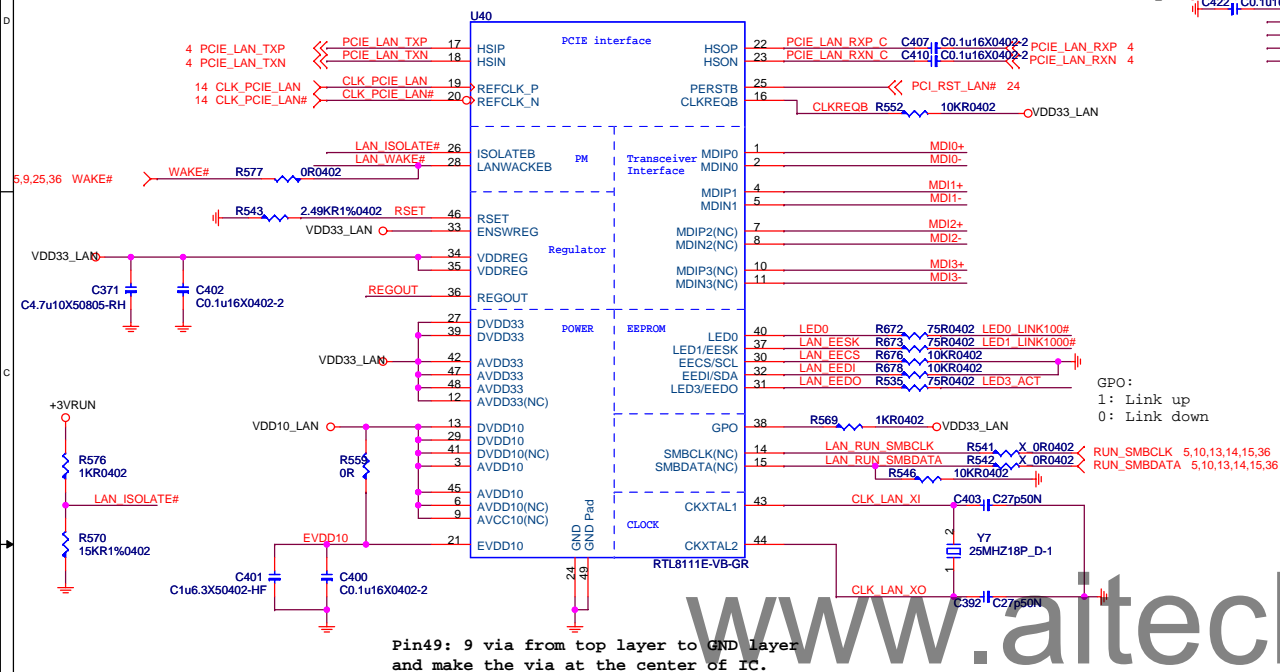
VGA INPUT

From D-SUB Conn

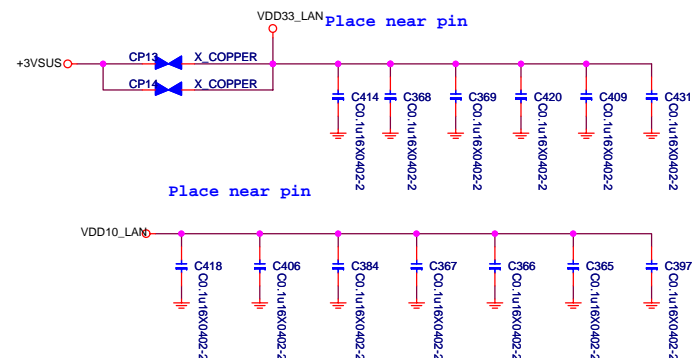


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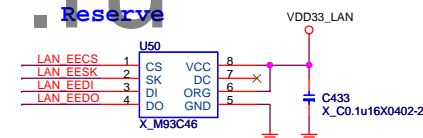
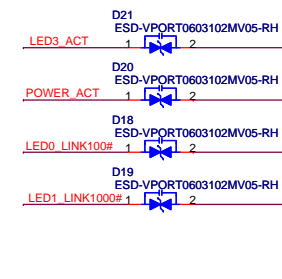
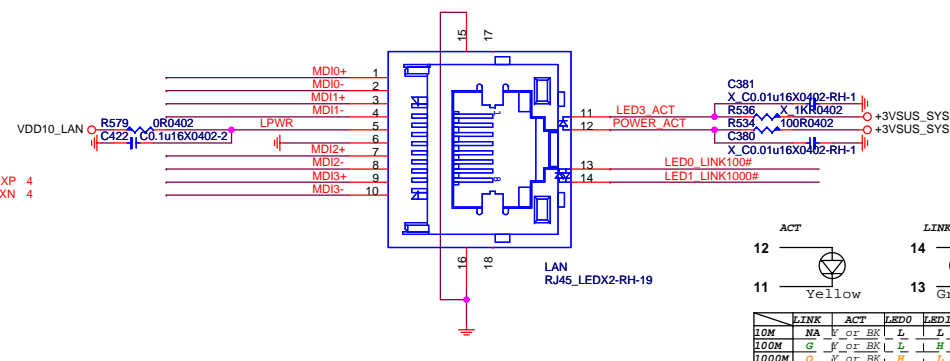
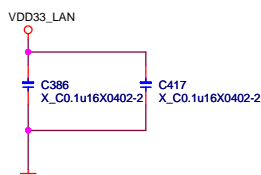
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			MS-7719	
Size	Document Description	Rev		
Custom	SCALER - VGA INPUT	0A		
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RTL8111E

3.3v Power on rise time : 1~100ms.



For EMI
(C73,C74,C75)



POWER Comparison

	3.3V	mW
10 M Idle/TxRx	87/172	287/568
100 M Idle/TxRx	112/165	370/545
ALDPS	60	198
D3 cold with link10M /without link	32/18	106/59.4

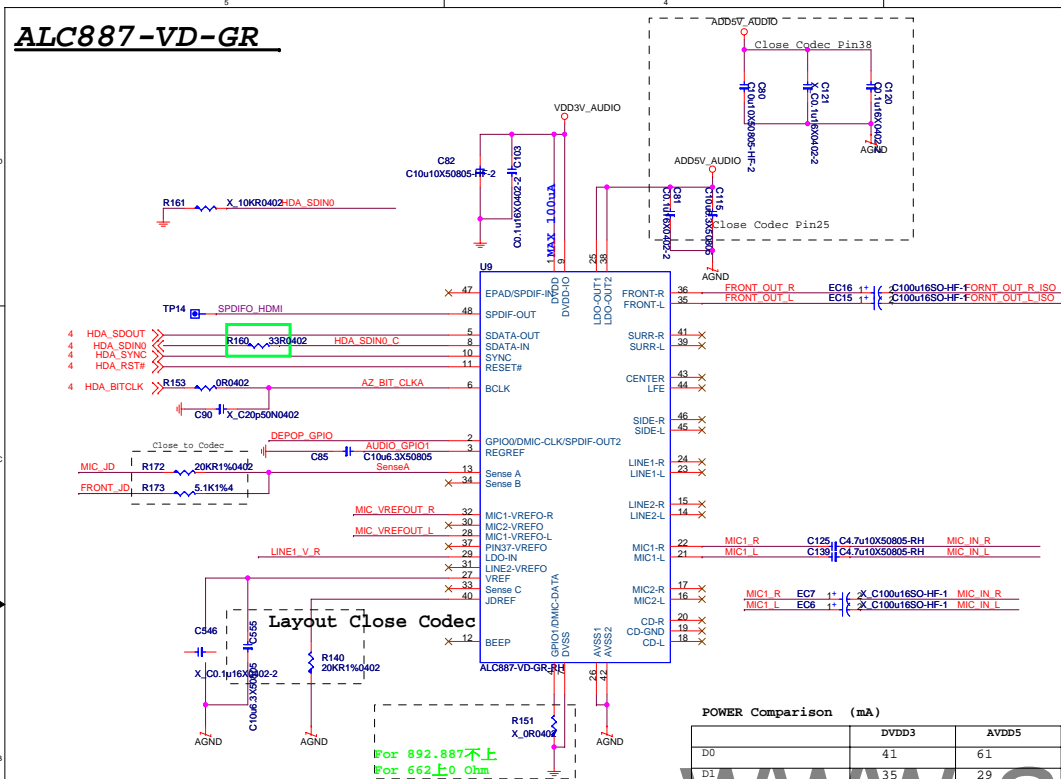


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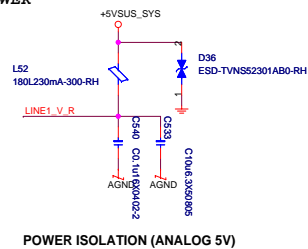
Size Custom	Document Description LAN - RTL8111E	Rev 0A
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ALC887-VD-GR

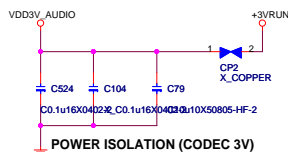


	DVDD3	AVDD5
D0	41	61
D1	35	29
D2	4.1	<1
D3	4.1	4
LINK Reset	3.1	14.31

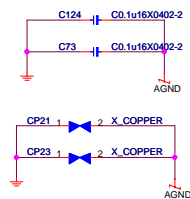
POWER



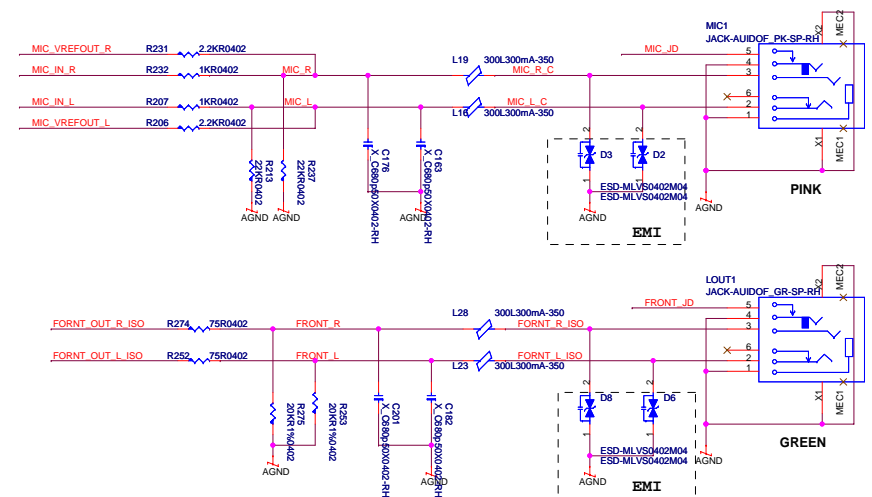
POWER ISOLATION (CODEC 3V)



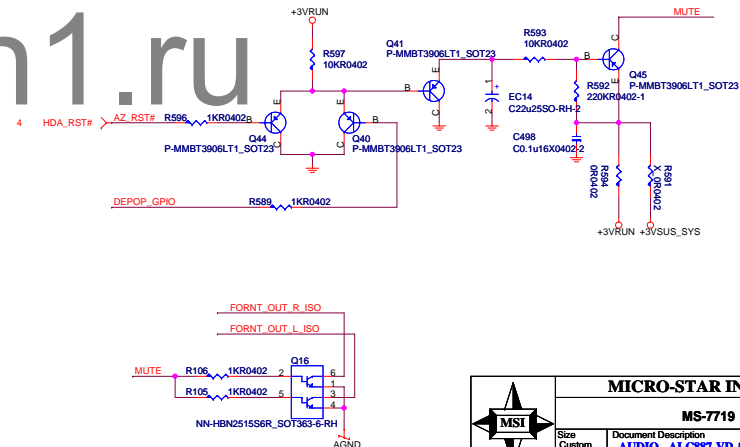
For EMI solution



AUDIO JACKS



ANTIPOP CIRCUIT

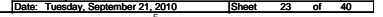


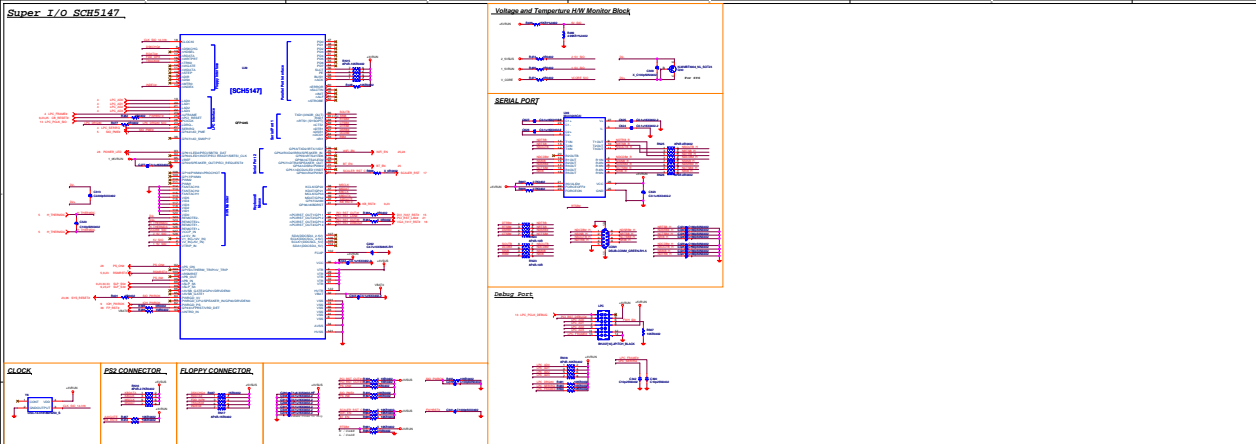
MICRO-STAR INT'L CO.,LTD

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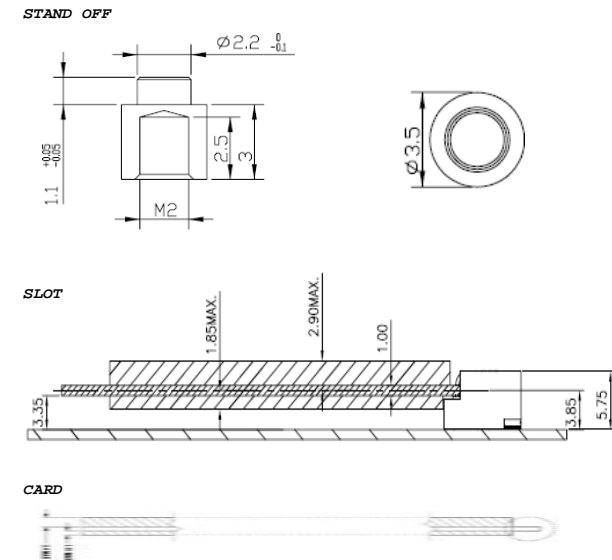
Size Custom	Document Description AUDIO - ALC887-VD & AMP
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For WiFi



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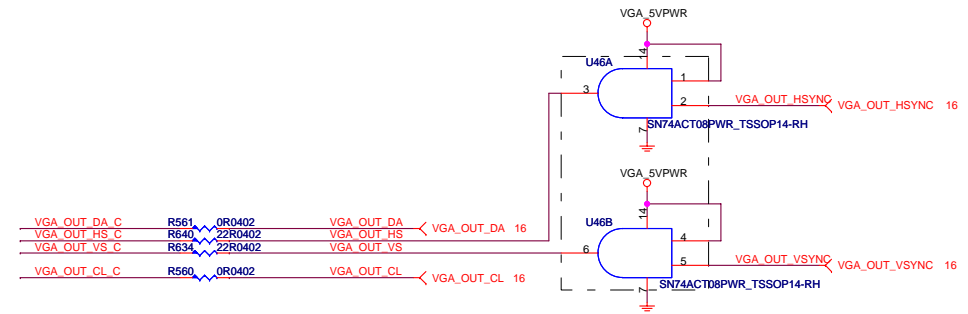
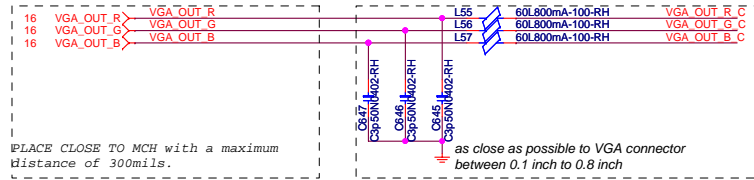


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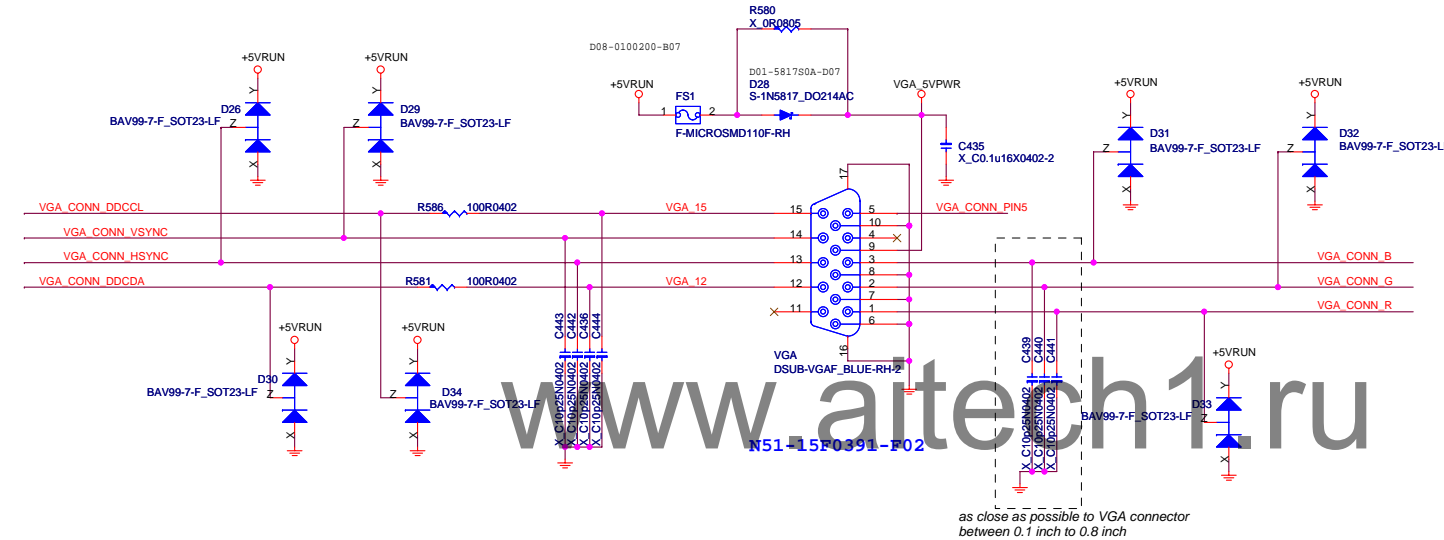
Size Custom	Document Description FAN& LED, TP	Rev 0A
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VGA CONNECT

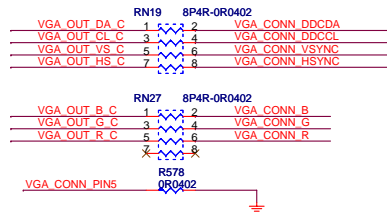
21.5" For Input
40" For Output



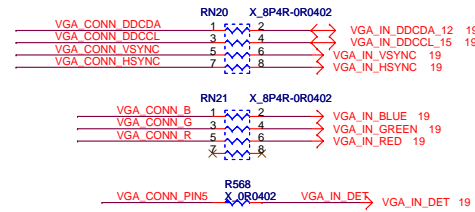
5.0 x 6.4 x 1.2 Millimeters



FOR SDVO TO RGB_OUT

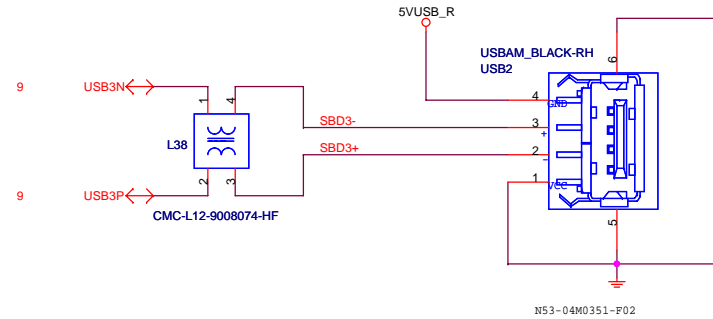
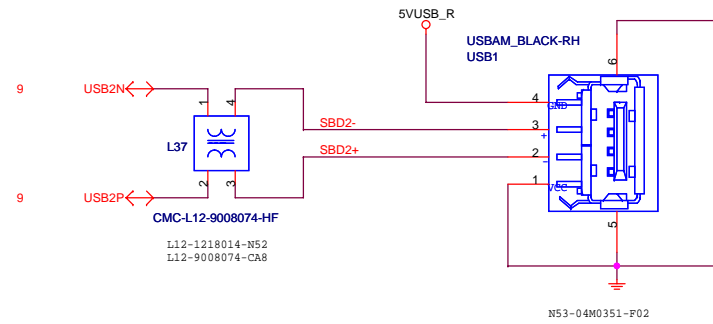
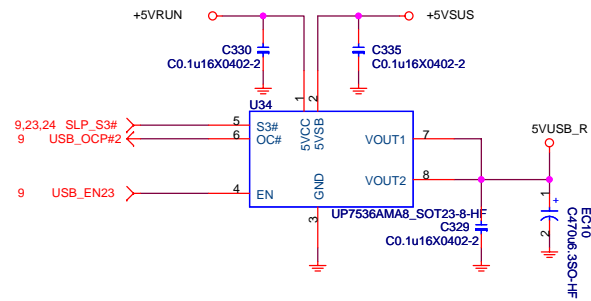


FOR RGB_IN TO LVDS

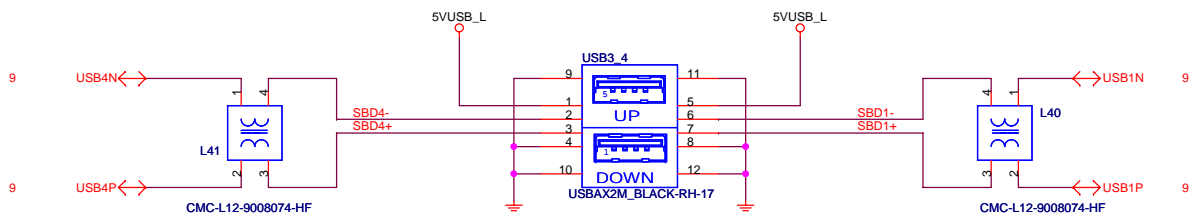
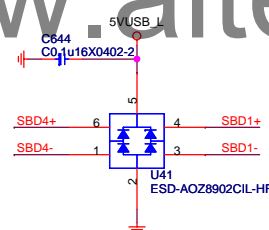
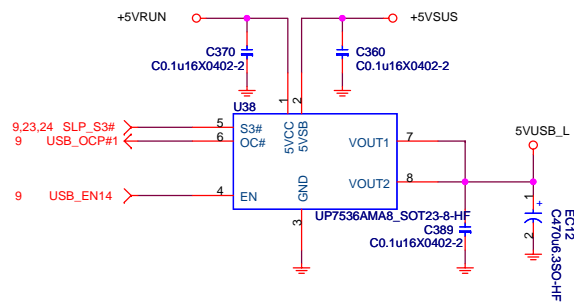


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MS-7719			
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Custom	VGA Conn	0A	
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USB CONNECT



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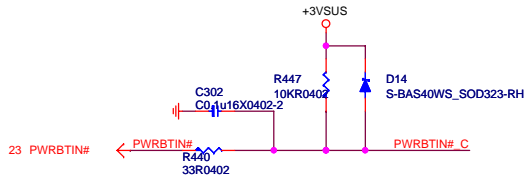
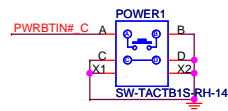
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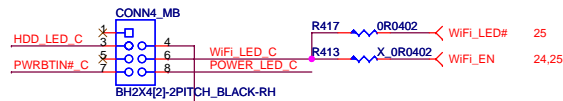
Size	Document Description	Rev
Custom	USB Conn	0A
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CONNECTOR HEADER

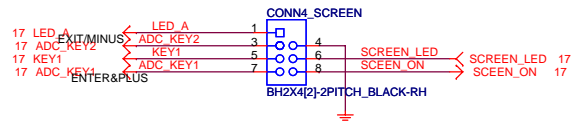
KEYPAD



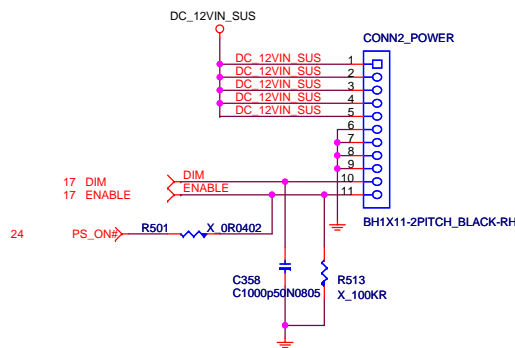
Conn4-1	MSI
1. POWER_BTN	1_7.NC
2. POWER_LED	2_8.X
3. NC	3_5.HDD_LED
4. WIFI_LED	4_6.GND
5. HDD_LED	5_3.NC
6. GND	6_4.WIFI_LED
7. NC	7_1.POWER_BTN
8. X	8_2.POWER_LED



Conn4-2	MSI
1. ADC_KEY1	1_7.LED_A(Reserve)
2. SCREEN ON/OFF	2_8.X
3. KEY1(Reserve)	3_5.ADC_KEY2
4. SCREEN_LED	4_6.GND
5. ADC_KEY2	5_3.KEY1(Reserve)
6. GND	6_4.SCREEN_LED
7. LED_A(Reserve)	7_1.ADC_Key1
8. X	8_2.SCREEN ON/OFF



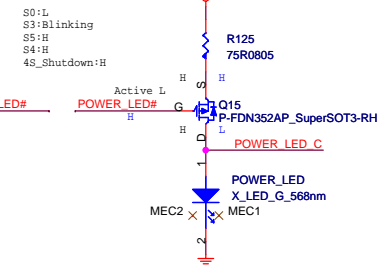
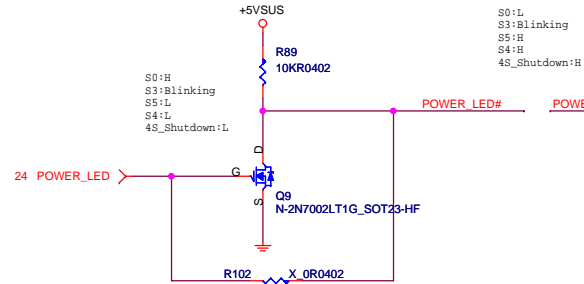
POWER INPUT



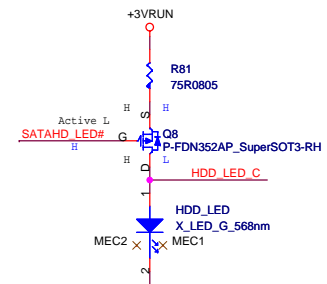
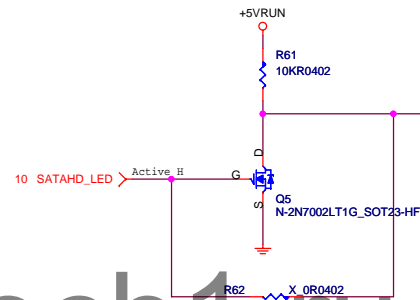
For EMI

HDD_LED C	C281	C0.1u16X0402-2
WIFI_LED C	C84	C0.1u16X0402-2
POWER_LED C	C291	C0.1u16X0402-2
SCREEN_LED	C295	C0.1u16X0402-2
PWRBTN# C	C307	C0.1u16X0402-2
SCREEN ON	C337	C0.1u16X0402-2
LED_A	C310	X C0.1u16X0402-2
ADC_KEY2	C318	C0.1u16X0402-2
KEY1	C188	X C0.1u16X0402-2
ADC_KEY1	C340	C0.1u16X0402-2

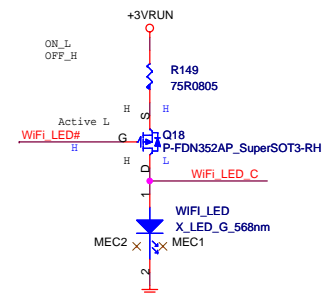
POWER_LED



HDD_LED



WIFI_LED

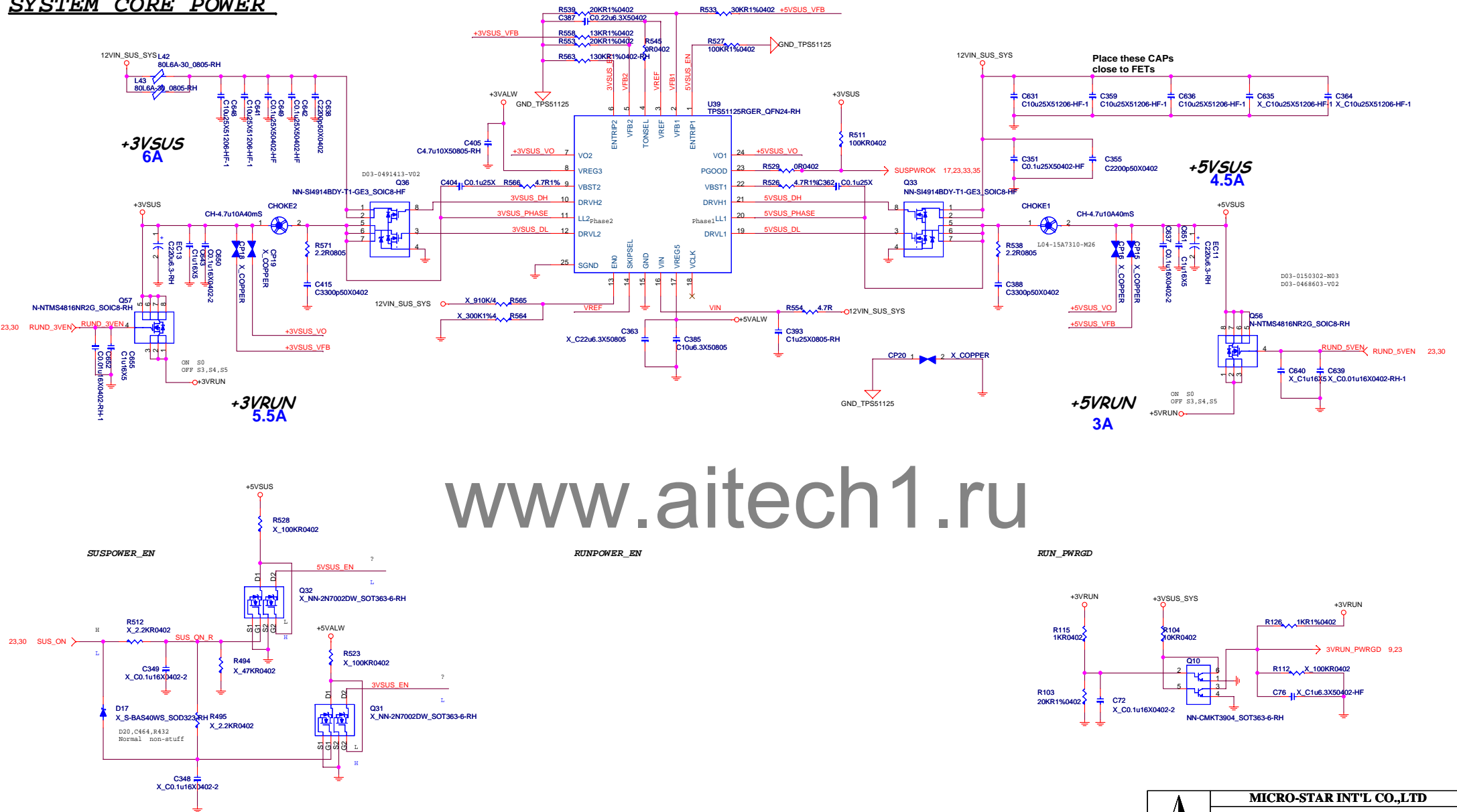


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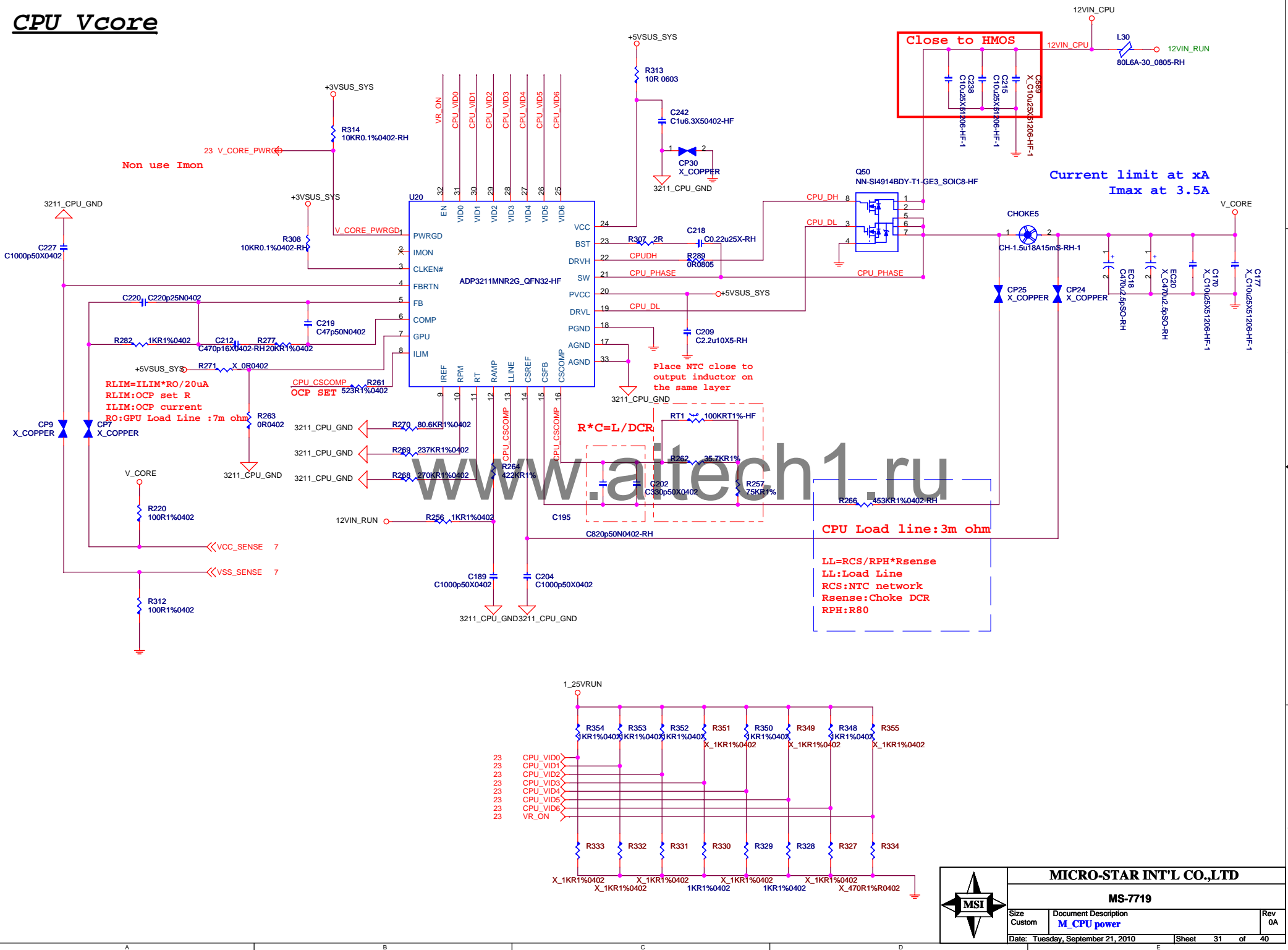
Size	Document Description	Rev
Custom	Power/Keypad Conn	0A
Date:	Tuesday, September 21, 2010	Sheet 28 of 40

SYSTEM CORE POWER

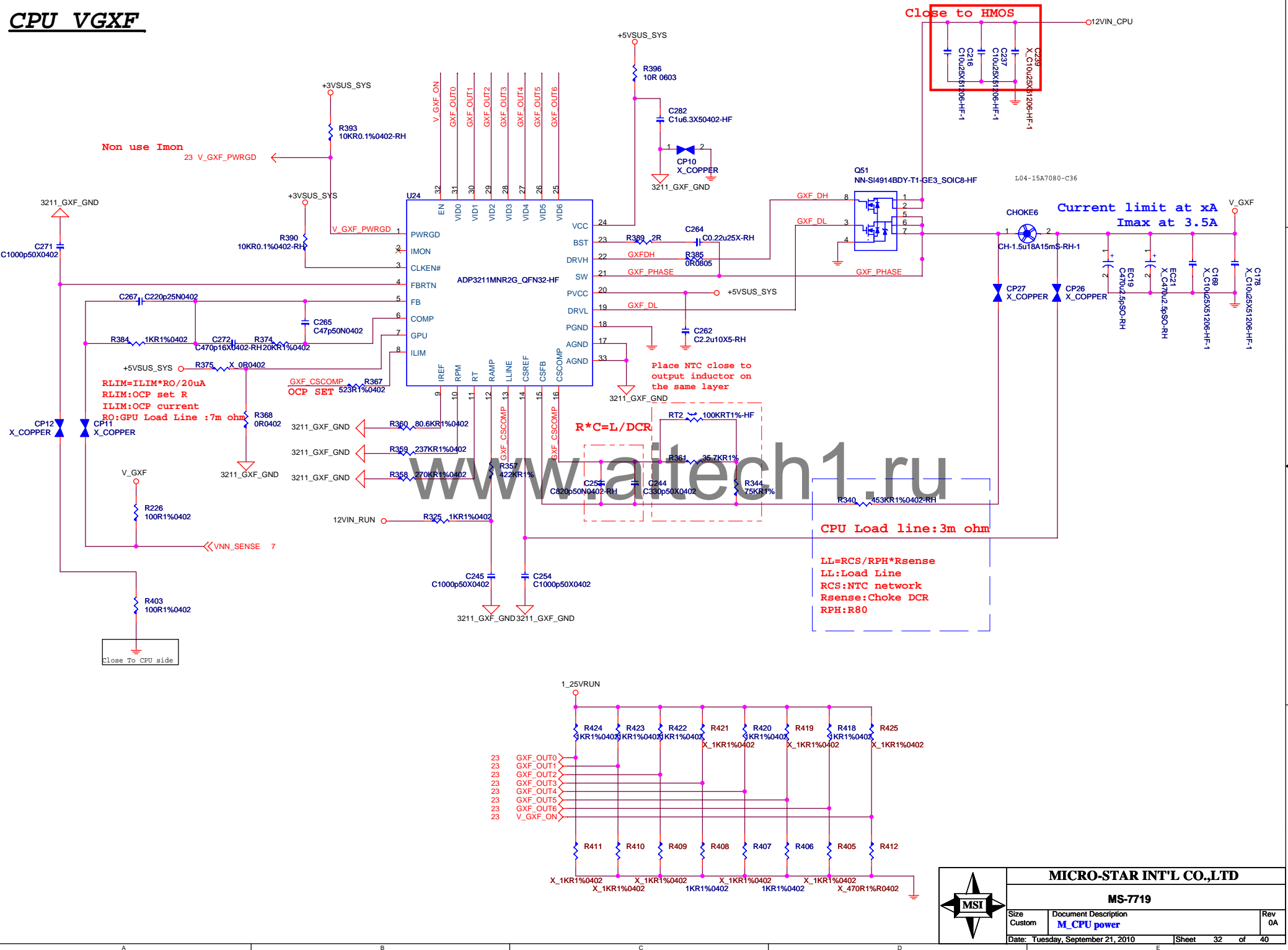


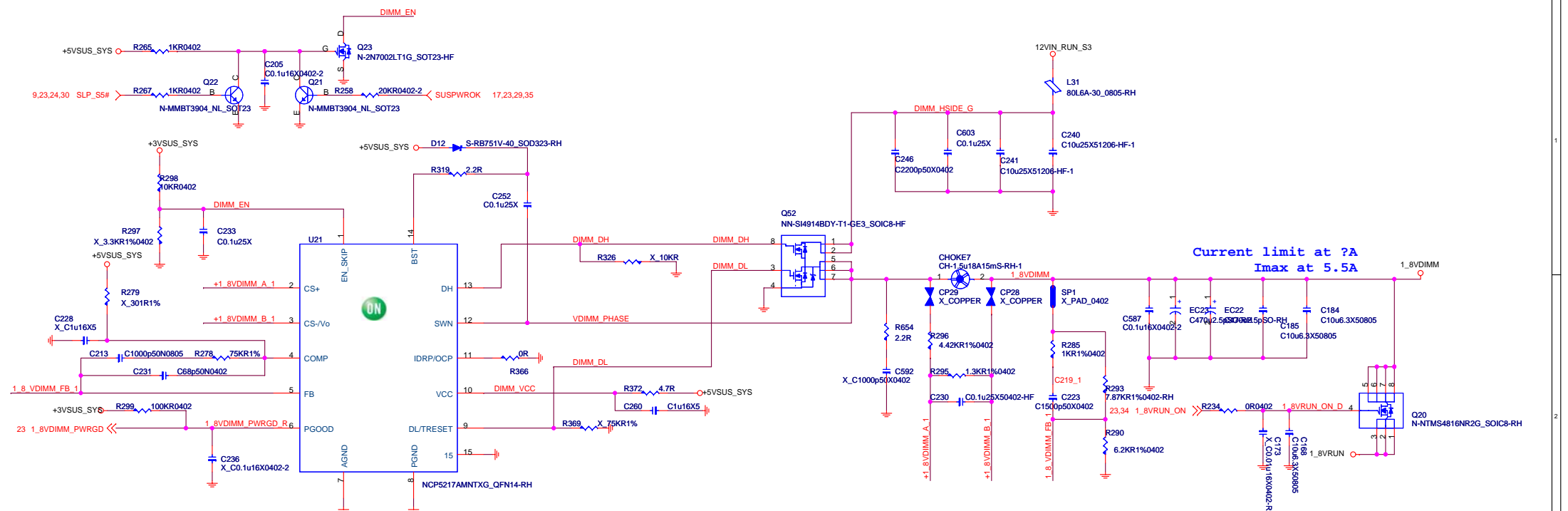
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MS-7719			
Size	Document Description	Rev	
Custom	System Power	0A	
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CPU Vcore

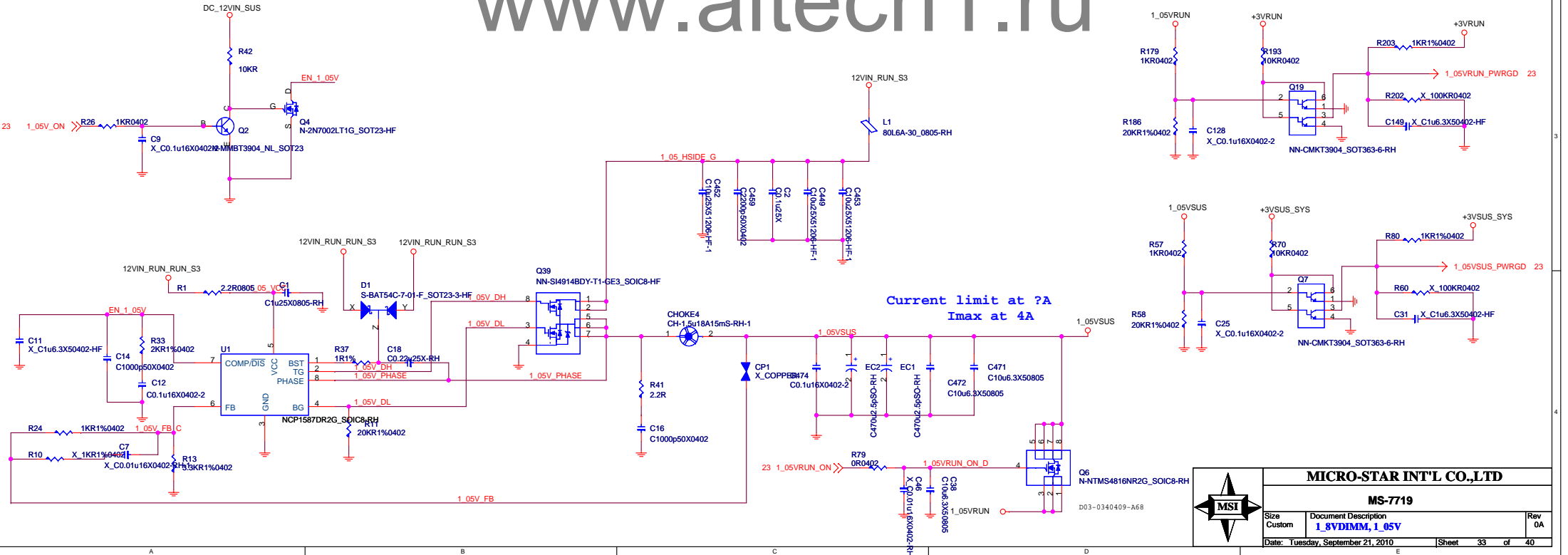


CPU VGXF

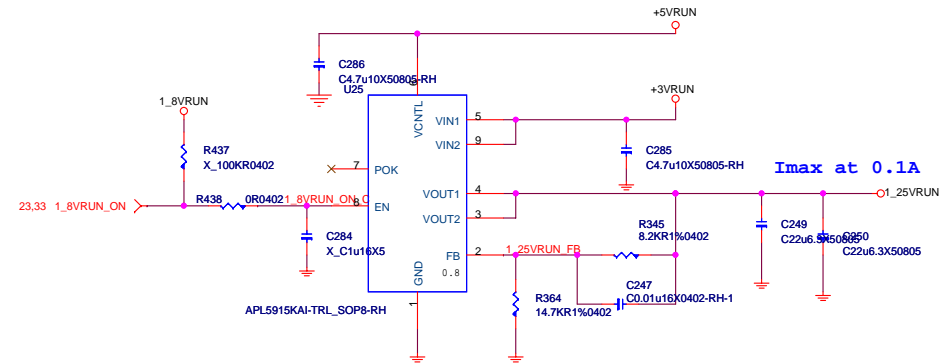
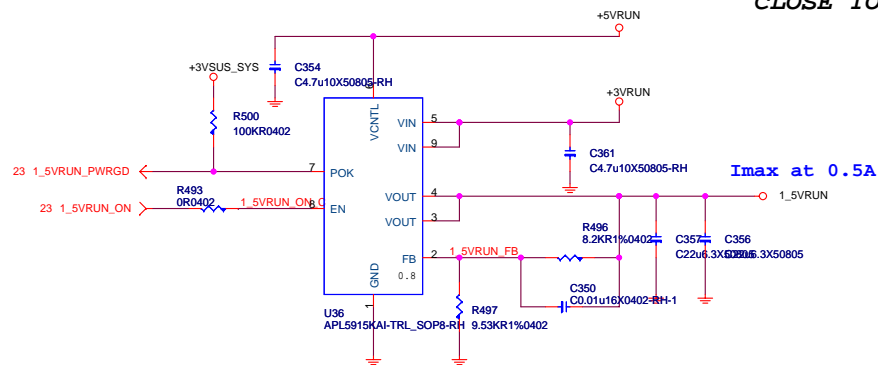




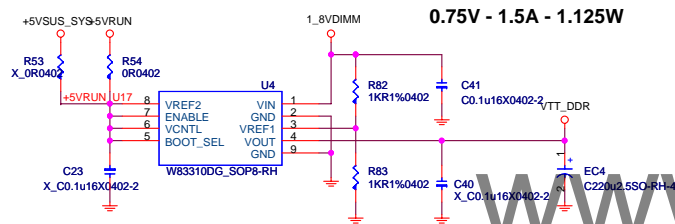
www.aitech1.ru



CLOSE TO CPU



DDRIII Termination Power



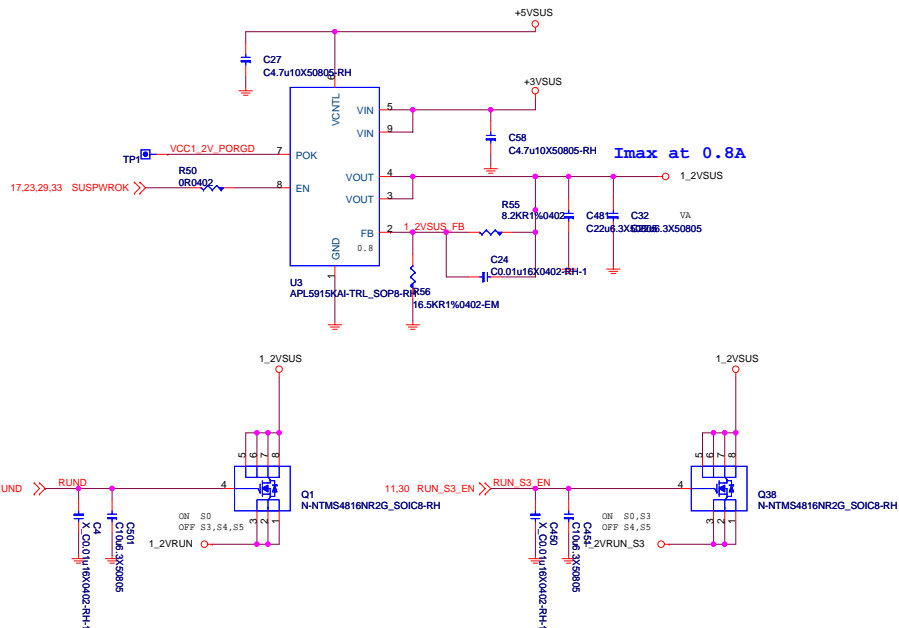
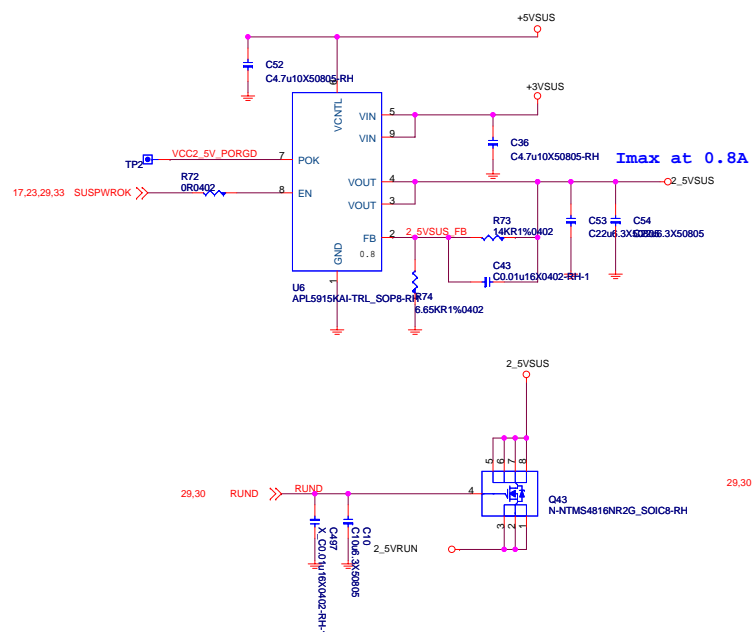
AVL: I31-0771102-U33 (UP7711)



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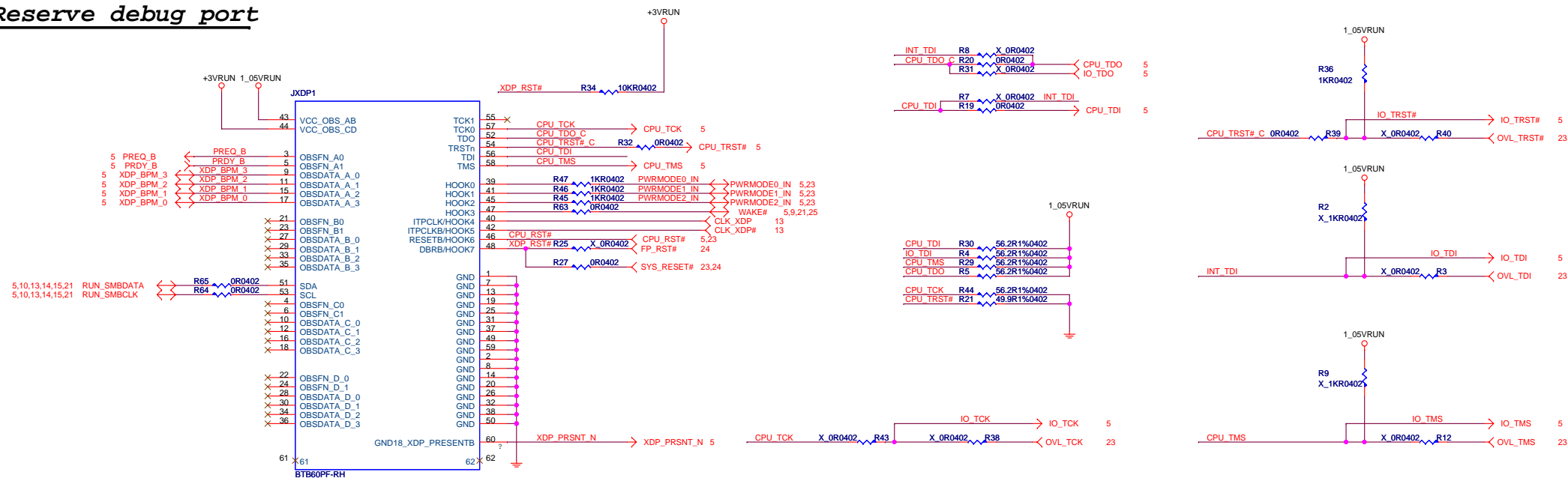
Size	Document Description	Rev
Custom	1.5VRUN,1.25VRUN	0A
Date:	Tuesday, September 21, 2010	Sheet 34 of 40



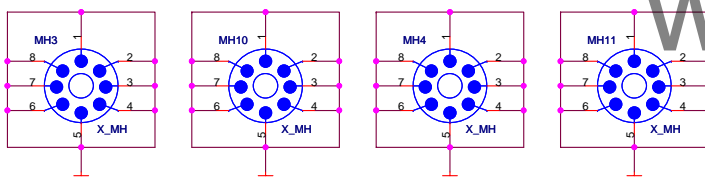
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MS-7719		
Size	Document Description	Rev
Custom	IOH 1.2V, 2.5V	0A
Date: Tuesday, September 21, 2010		Sheet 35 of 40

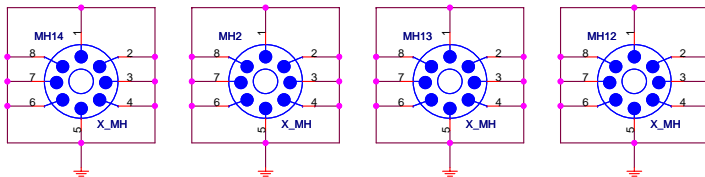
Reserve debug port



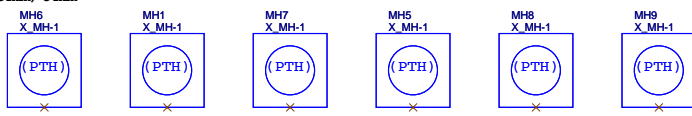
3.5mm/6mm



4.5mm/7mm



3mm/6mm




Simulation



Inner Layer

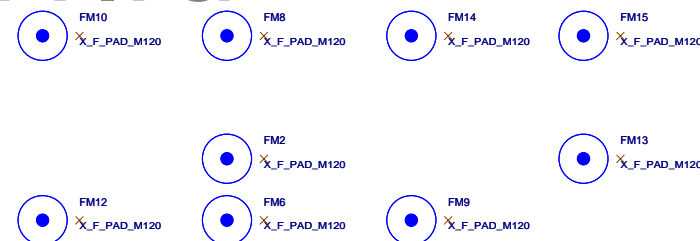
Inner Layer


 SIP1
 SIM4
 X_PIN1*2
 Bottom Layer

50 ohm 4/4

Optics Orientation Holes

Optical Fiducial Marks-120



STAND OFF FOR MINI PCIE



Holes_R177D91

E2B-1634020-A89



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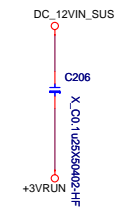
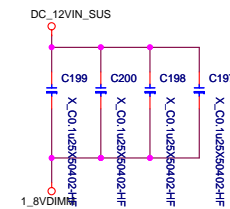
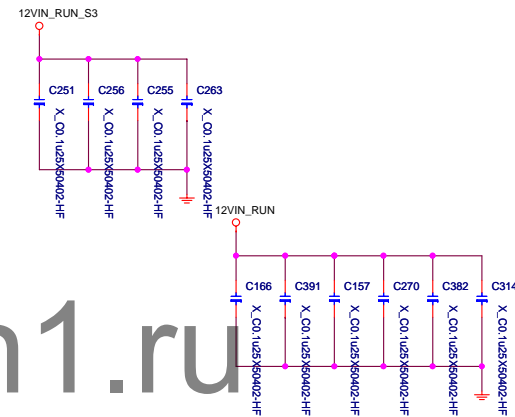
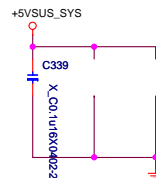
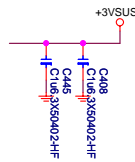
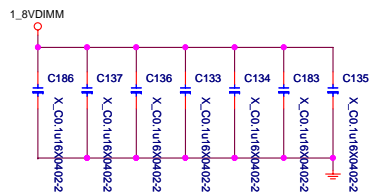
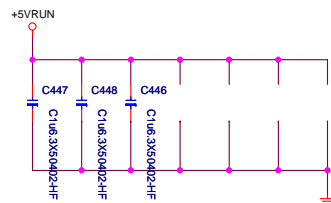
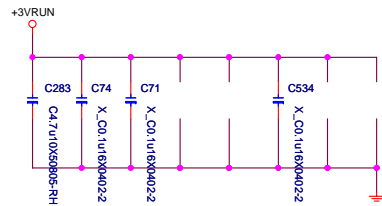
Size Custom	Document Description XDP/ ME part	Rev 00
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P80-077190A-T53

E2M-4112511-CA7

H: 3.7mm



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Size		Document Description		Rev
Custom		Manual Part		0A
Date: Monday, September 27, 2010		Sheet 37 of 40		